

# Strike

**AX01 Build**

**MS14  
2010.10.06**

**INVENTEC**

TITLE			
Strike			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	X01
SHEET			
1		of	58

# 1. Schematic Page Description :

## MS14 Schematic Ver : X01

01. Title	16. Processor_DDR3	31. PCH_GND	46. N12M/DACA/DACB
02. Schematic Page DESCR	17. Processor_Power	32. KBC_IT8518E	47. N12M/IFPAB/IFPCD/IFPEF
03. Block Diagram	18. Processor_Power	33. CRT	48. N12M/I2C/THERM
04. Power Block Diagram	19. Processor_GND	34. WEB_CAM/LVDS	49. N12M/STARP/OSC
05. Annotations	20. THERMAL/FAN	35. HDMI	50. DDR3 VRAM
06. PWR_Adaptor in/Charge	21. DDR3 SDRAM SO-DIMM 0/1	36. HDD/ODD	51. GPU Power-1
07. PWR_CPU Core Power	22. DDR3 SDRAM SO-DIMM 1/1	37. CARD_READER	52. GPU Power-2
08. PWR_1.5V/1.5VS/DDR_PWR	23. PCH_RTC,SATA,SPI,IHDA	38. Audio_ALC269Q	53. USB_Board
09. PWR_1.05V/0.85V	24. PCH_PCI_e,I2C,CLK	39. AUDIO CNN	54. LAN_RTL8111E
10. PWR_5VLA/3VLA/5VACP	25. PCH_DMI,FDI,Power_CTRL	40. Charge USB	55. USB CNN
11. PWR_1.8VS/3VS/5VS	26. PCH_DMI,MISC,LVDS,CRT	41. LED	56. PWR_SW_Board
12. PWR_5VA/SCREW/IO CNN	27. PCH_LVDS,CRT,HDMI	42. I/O CNN	57. PWR_SW CNN
13. POWER SEQUENCE	28. PCH_PCI,USB	43. WLAN,BT	58. GP_Board
14. Processor_DMI,FDI,PCI_e	29. PCH_GPIO,MISC	44. N12M/PCI-EXPRESS	59. GP CNN
15. Processor_THRM,MISC	30. PCH_POWER	45. N12M/FRAME_BUFFER	

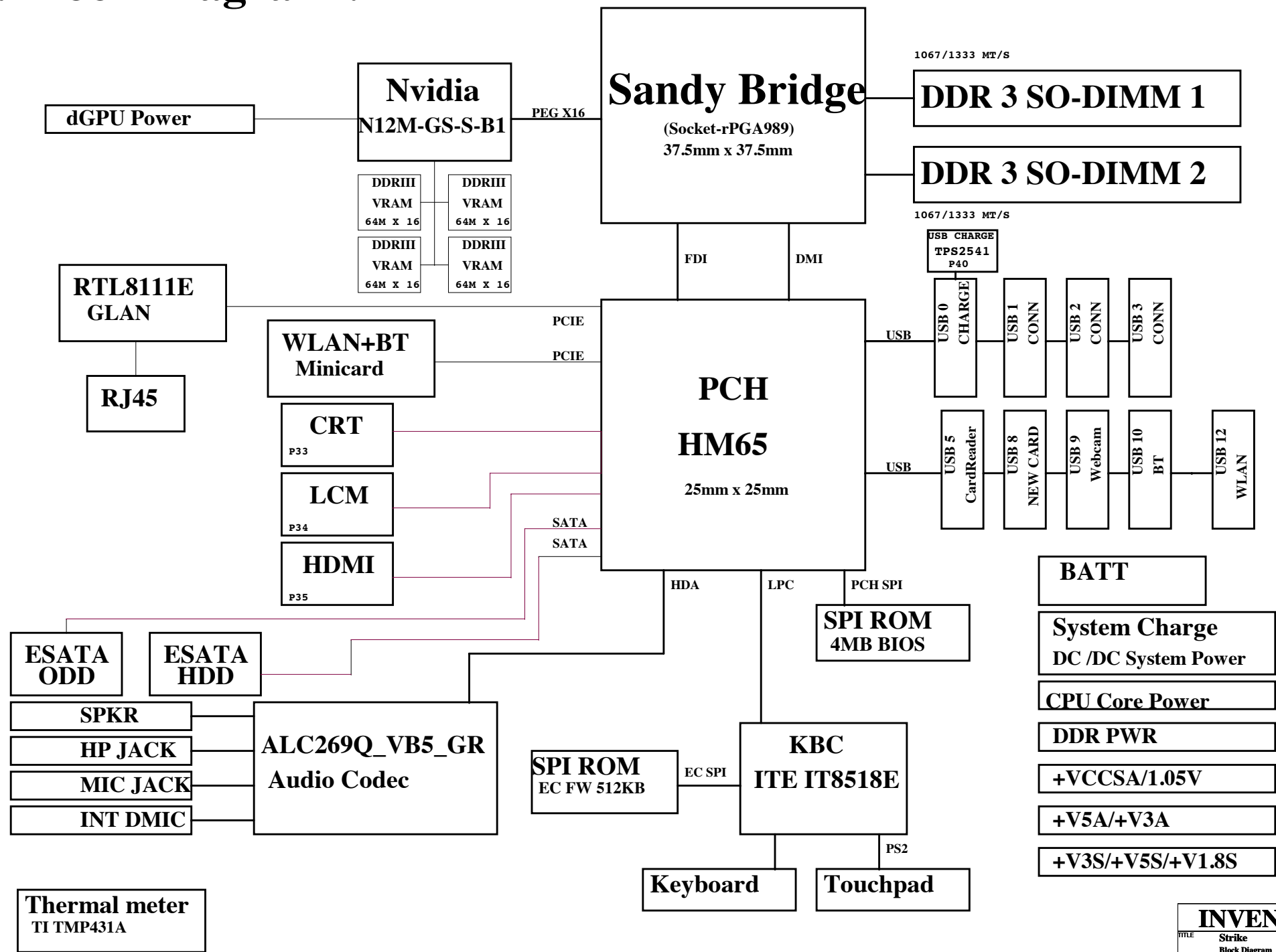
# 2. PCI & IRQ & DMA Description :

IDSEL	CHIP	PCIINT	CHIP	Interface	REQ	CHIP
None		None			None	

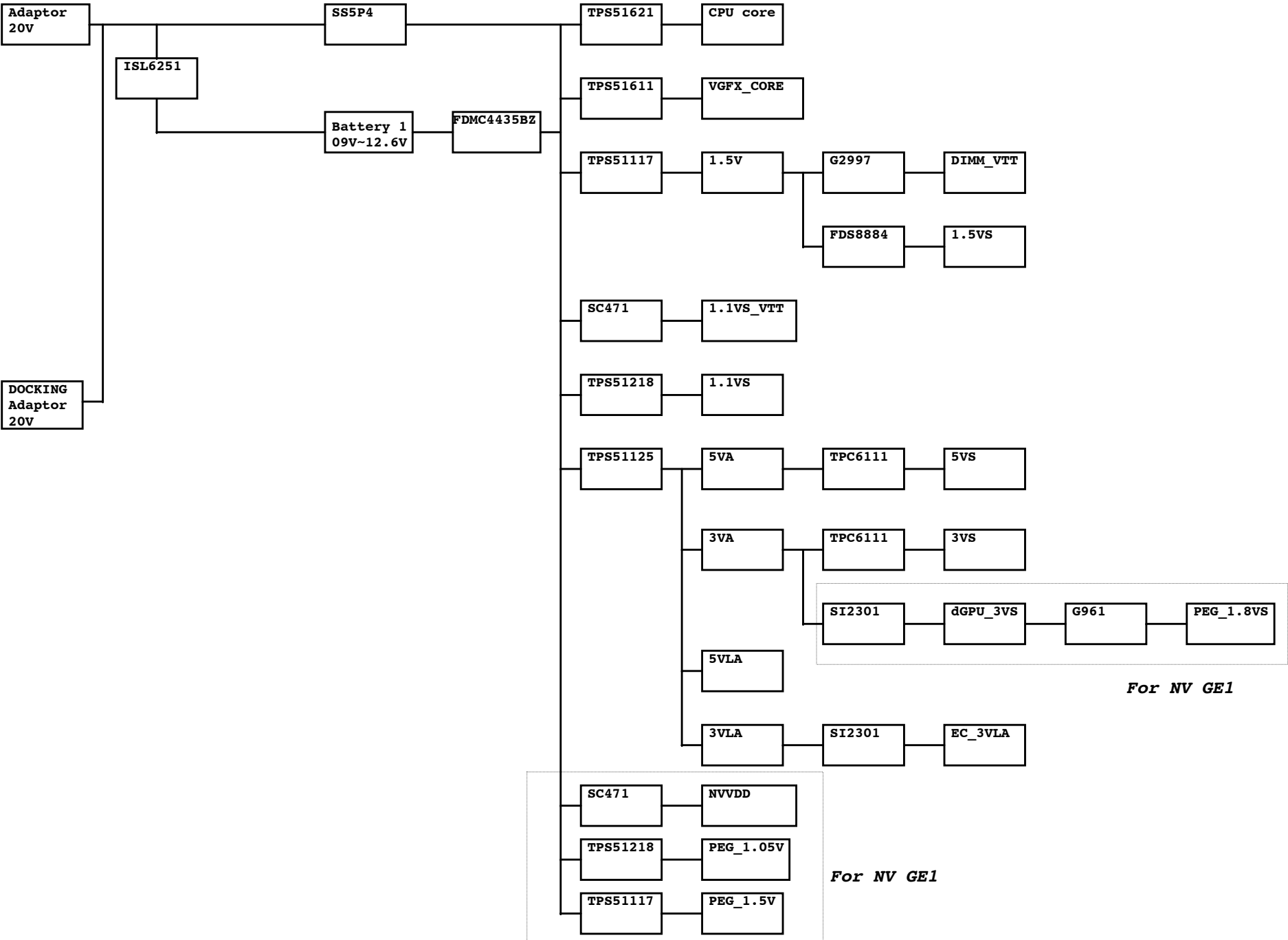
# 3. USB & PCI-Express & SATA Description :

USB Port	DEVICE	USB Port	DEVICE	PCI-E	DEVICE	SATA	DEVICE
Port 0	System (ESATA)	Port 7	Bluetooth	Port 1	New Card	Port 1	HDD
Port 1	System	Port 8		Port 2	Docking	Port 2	E-SATA
Port 2	System	Port 9	Web Cam	Port 3	Mini Card(WLAN)	Port 4	BAY
Port 3	System	Port 10		Port 4	Mini Card(3G)	Port 5	None
Port 4	CardReader	Port 11	FingerPrint	Port 5	Mini Card(ROBSON)		
Port 5		Port 12		Port 6	Giga-LAN		
Port 6		Port 13	3G				

### 3. Block Diagram :



# Power Block Diagram :



For NV GE1

For NV GE1

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TITLE				
Strike				
Power Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
Custom	CS	CS-131	4	X01
SHEET				

# 4. Net name Description :

## Voltage Rails

DCIN	Primary DC system power supply
3VLA	3.3V always on power rail by DCIN
5VLA	5.0V always on power rail by DCIN
EC_3VLA	3.3V always on power rail by 5VAUXON
3VA	3.3V always on power rail by LATCH_ON
5VA	5.0V always on power rail by LATCH_ON
3VM	3.3V power rail by SUSM#
1.05VM	1.05V switched power rail by SUSM#
1.5V	1.5V switched power rail by SUSC#
1.8V	1.8V power rail by SUSC#
3VS	3.3V power rail by SUSB#
5VS	5.0V power rail by SUSB#
1.5VS	1.5V power rail by SUSB#
1.05VS	1.05V power rail by SUSB#
PWR_DIMM_VTT	0.75V DDR Termination Voltage by SUSB#
VGFX_CORE	1.05V power rail for UMA by SUSB#
PEG_1.8VS	1.8V switched power rail for NB9x by SUSB#
PEG_PEX_1.1VS	1.1V switched power rail for NB9x by SUSB#
PEG_NVDD	Variable switched power rail for NB9x by SUSB#

Vcore\_CPU Core switched power rail for CPU

## Part Naming Conventions

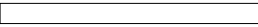







C	= Capacitor	Q	= Transistor
CN	= Connector	R	= Resistor
D	= Diode	RP	= Resistor Pack
F	= Fuse	U	= Arbitrary Logic Device
L	= Inductor	Y	= Crystal and Osc

## Name Suffix

#	= Active Low signal
NU	= No Stuff

# 5. Board Stack up Description

## PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

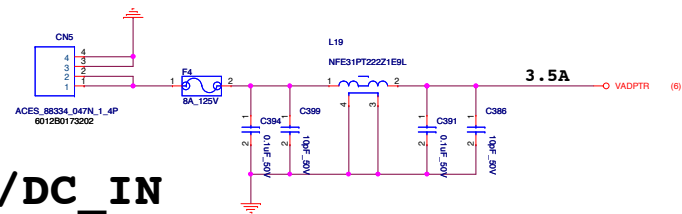
	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	36A
1.05VS	Penryn: AGTL+ termination Cantiga GM: Core Cantiga GM: PCIE Cantiga GM:Core+IMEL+HSIO Cantiga GM:VCC_GMCH Cantiga GM:VCCA_SM_CK and NCTF Cantiga GM:VCC_DMI Cantiga GM:VCCA_SM Cantiga GM:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn PLL Cantiga GM: QDAC Cantiga GM: LVDS Cantiga GM: TVDAC Cantiga GM: Various PLLS analog supply Cantiga GM: VCC_SM_CK Cantiga GM: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GM: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIIIDDRIII Terminator:		0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GM: HV CMOS Cantiga GM: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS397BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:82567LM Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 1.0V and 1.8V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A Each 1A
5VS	Cardreader: GL827 Azalia Codec: ALC262 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB and ESATA	5VA 5VA	1.5A 2A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

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Strike Annotations

SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	X01
SHEET	5	of	58



**Battery CNN**

(32) BATTERY1\_IN

(10,12) 5VLA

(32,6) BATT\_CLK  
(32,6) BATT\_DATA

(46) +VBDC

U1: LITTLEFUSE\_R451015\_15A\_65V

10A

U2: EZJ20V500AA-1

U3: EZJ20V500AA-1

U4: EZJ20V500AA-1

U5: EZJ20V500AA-1

U6: EZJ20V500AA-1

U7: EZJ20V500AA-1

U8: EZJ20V500AA-1

U9: EZJ20V500AA-1

U10: EZJ20V500AA-1

U11: EZJ20V500AA-1

U12: EZJ20V500AA-1

U13: EZJ20V500AA-1

U14: EZJ20V500AA-1

U15: EZJ20V500AA-1

U16: EZJ20V500AA-1

U17: EZJ20V500AA-1

U18: EZJ20V500AA-1

U19: EZJ20V500AA-1

U20: EZJ20V500AA-1

U21: EZJ20V500AA-1

U22: EZJ20V500AA-1

U23: EZJ20V500AA-1

U24: EZJ20V500AA-1

U25: EZJ20V500AA-1

U26: EZJ20V500AA-1

U27: EZJ20V500AA-1

U28: EZJ20V500AA-1

U29: EZJ20V500AA-1

U30: EZJ20V500AA-1

U31: EZJ20V500AA-1

U32: EZJ20V500AA-1

U33: EZJ20V500AA-1

U34: EZJ20V500AA-1

U35: EZJ20V500AA-1

U36: EZJ20V500AA-1

U37: EZJ20V500AA-1

U38: EZJ20V500AA-1

U39: EZJ20V500AA-1

U40: EZJ20V500AA-1

U41: EZJ20V500AA-1

U42: EZJ20V500AA-1

U43: EZJ20V500AA-1

U44: EZJ20V500AA-1

U45: EZJ20V500AA-1

U46: EZJ20V500AA-1

U47: EZJ20V500AA-1

U48: EZJ20V500AA-1

U49: EZJ20V500AA-1

U50: EZJ20V500AA-1

U51: EZJ20V500AA-1

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U56: EZJ20V500AA-1

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U86: EZJ20V500AA-1

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U92: EZJ20V500AA-1

U93: EZJ20V500AA-1

U94: EZJ20V500AA-1

U95: EZJ20V500AA-1

U96: EZJ20V500AA-1

U97: EZJ20V500AA-1

U98: EZJ20V500AA-1

U99: EZJ20V500AA-1

U100: EZJ20V500AA-1

U101: EZJ20V500AA-1

U102: EZJ20V500AA-1

U103: EZJ20V500AA-1

U104: EZJ20V500AA-1

U105: EZJ20V500AA-1

U106: EZJ20V500AA-1

U107: EZJ20V500AA-1

U108: EZJ20V500AA-1

U109: EZJ20V500AA-1

U110: EZJ20V500AA-1

U111: EZJ20V500AA-1

U112: EZJ20V500AA-1

U113: EZJ20V500AA-1

U114: EZJ20V500AA-1

U115: EZJ20V500AA-1

U116: EZJ20V500AA-1

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U142: EZJ20V500AA-1

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U144: EZJ20V500AA-1

U145: EZJ20V500AA-1

U146: EZJ20V500AA-1

U147: EZJ20V500AA-1

U148: EZJ20V500AA-1

U149: EZJ20V500AA-1

U150: EZJ20V500AA-1

U151: EZJ20V500AA-1

U152: EZJ20V500AA-1

U153: EZJ20V500AA-1

U154: EZJ20V500AA-1

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U160: EZJ20V500AA-1

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U179: EZJ20V500AA-1

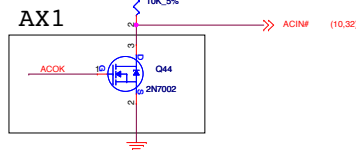
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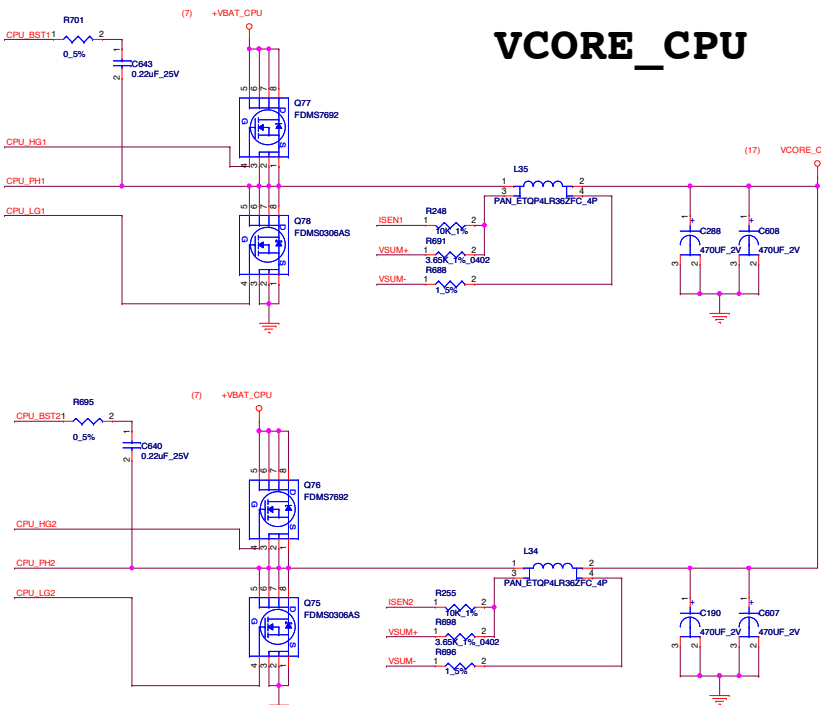
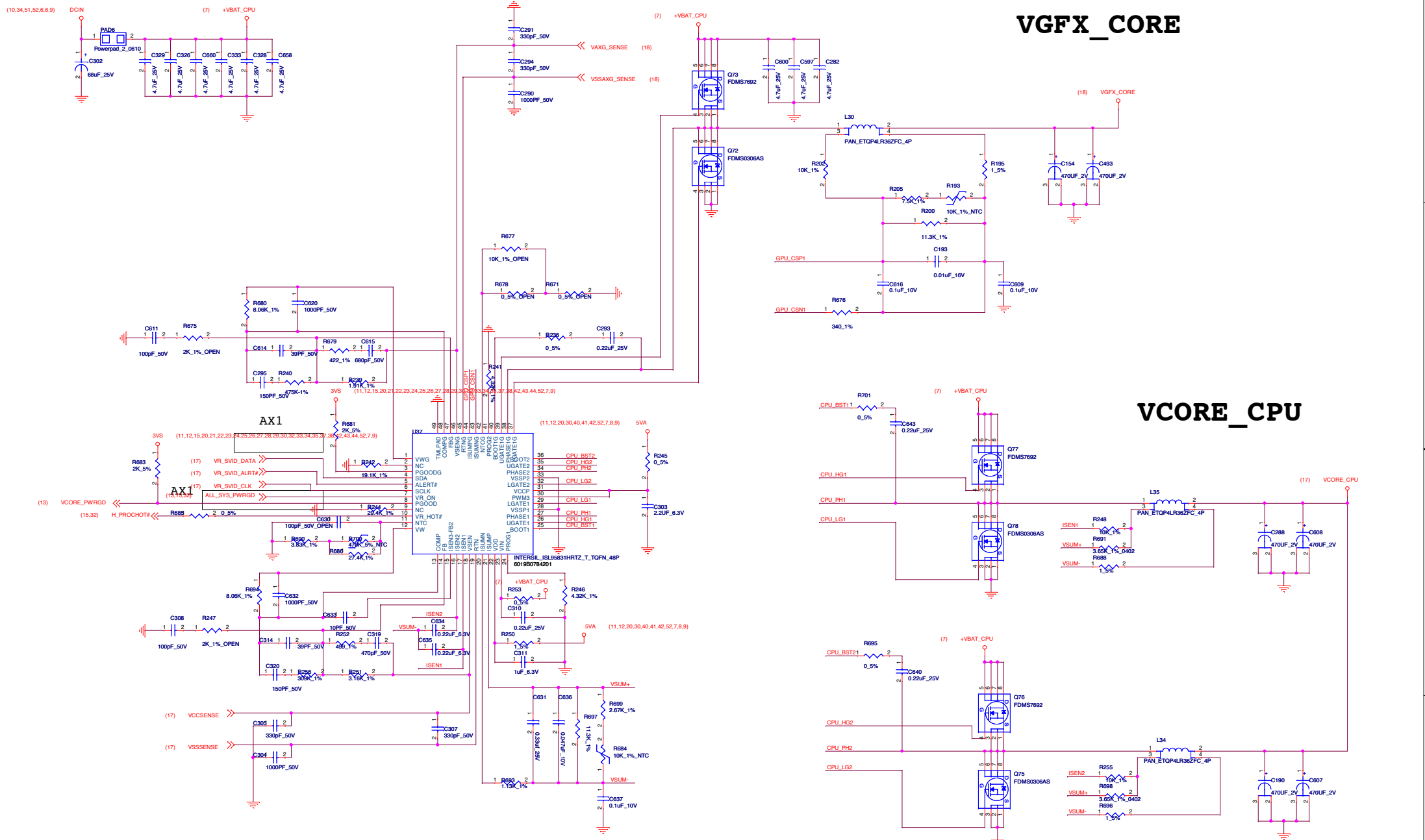
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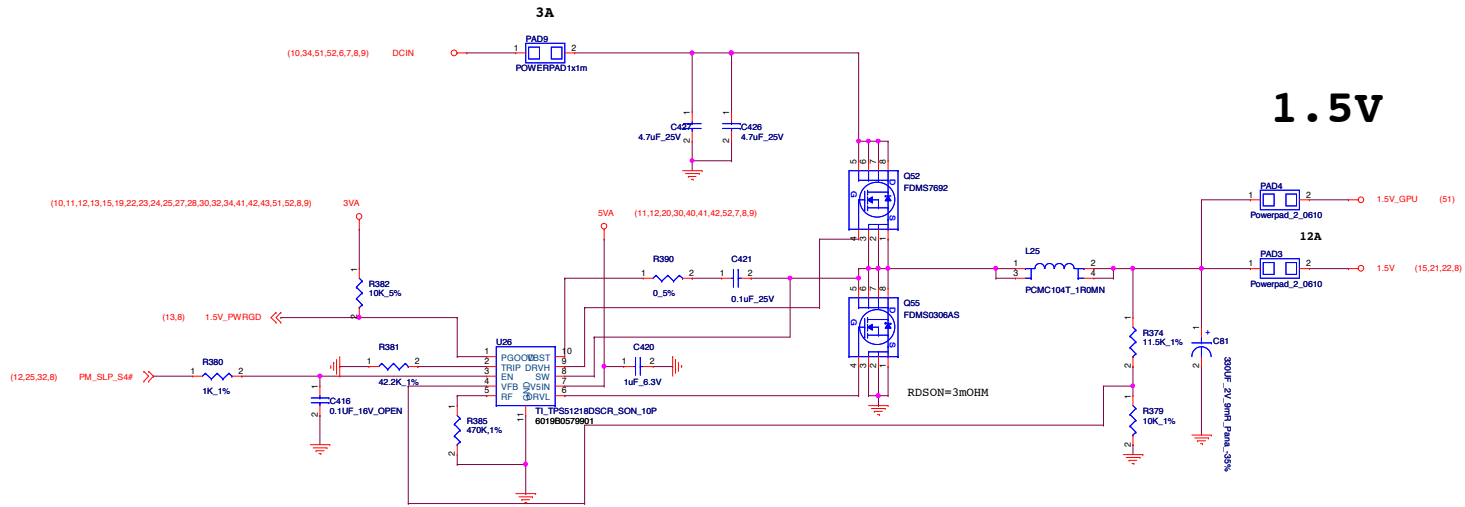
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U1

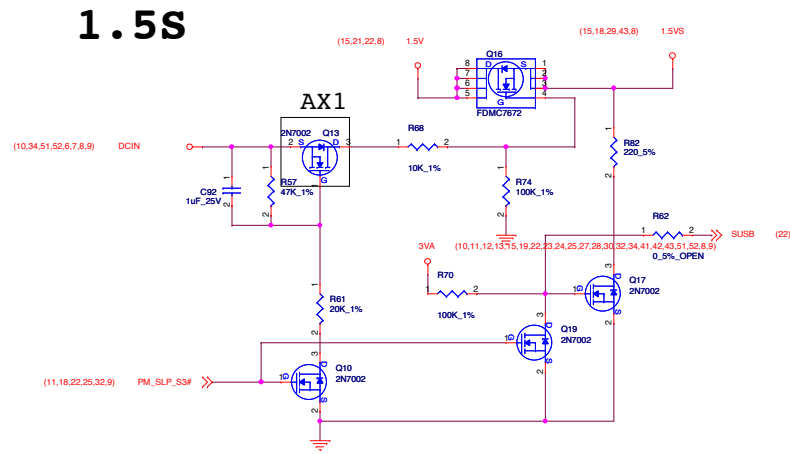




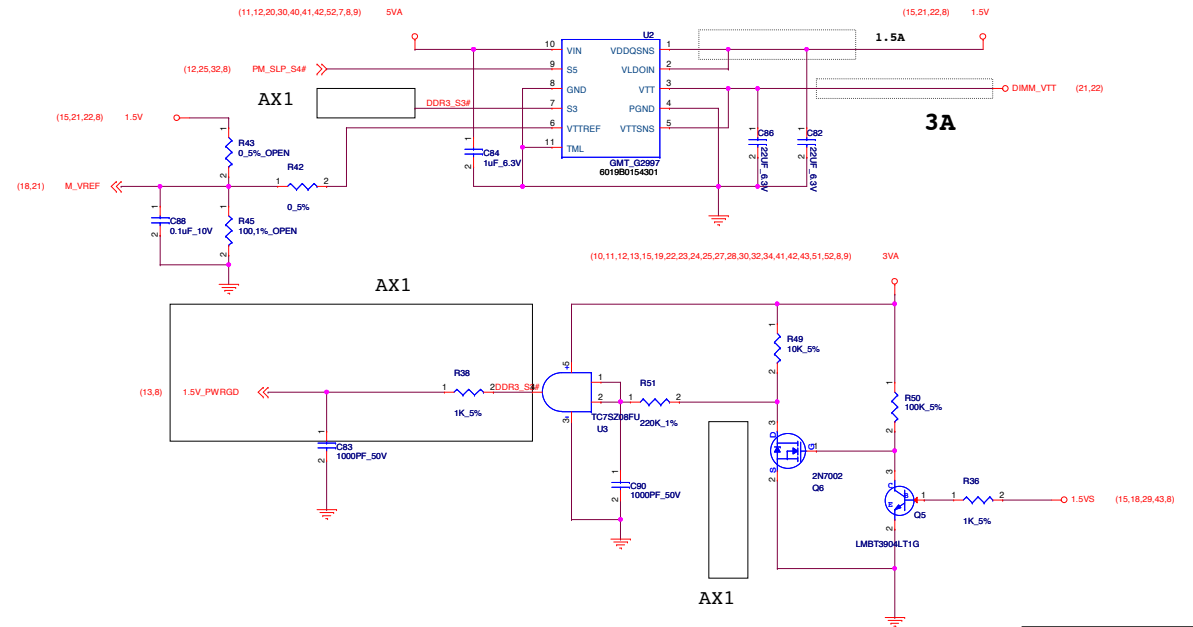


1.5V

DIMM\_VTT



1.5S

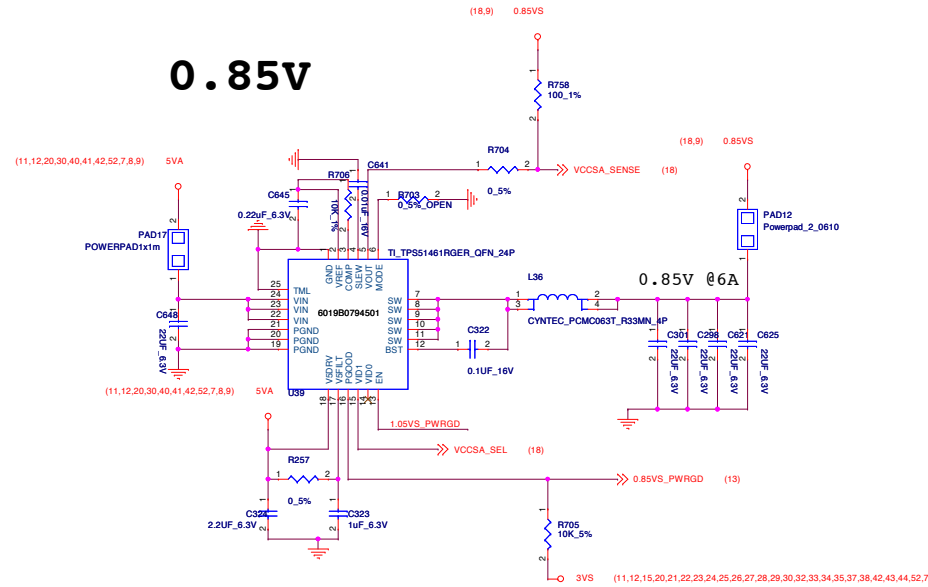


3A

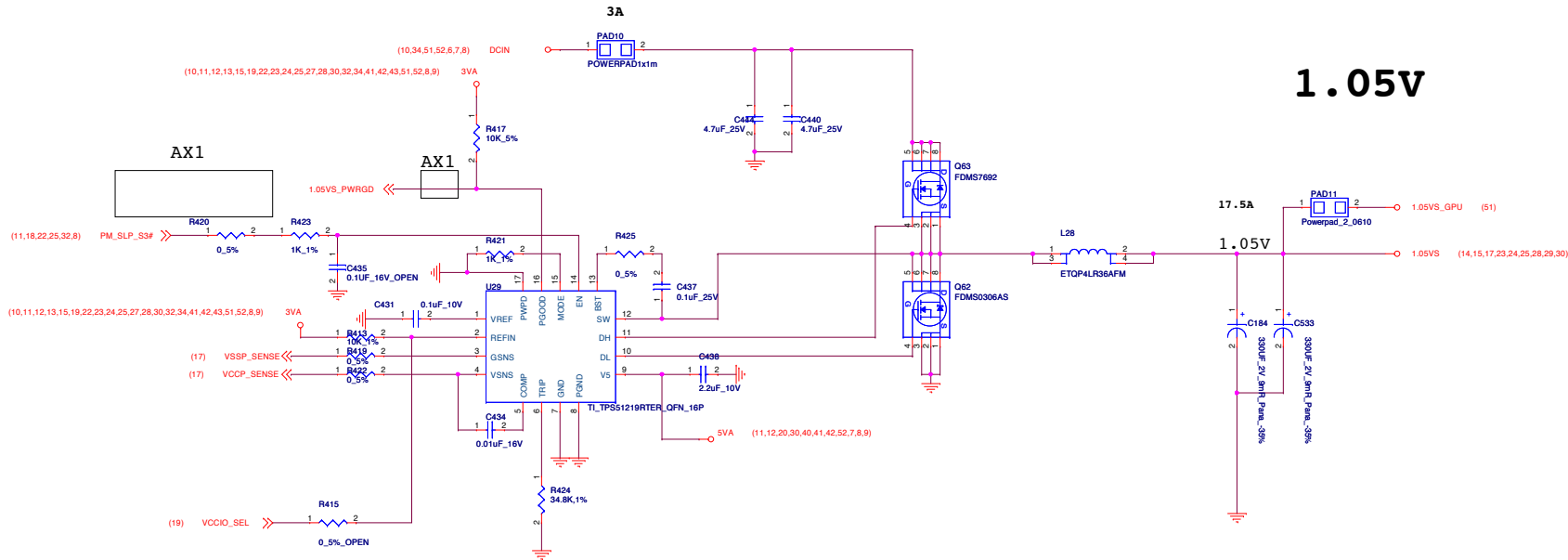
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<b>TITLE</b>			
<b>Strike</b>			
<b>DDR PWR</b>			
<b>SIZE</b>	<b>CODE</b>	<b>DOC. NUMBER</b>	<b>REV</b>
Custom	CS	CS-131	X01
SHEET 8 of 89			



0.85V



1.05V



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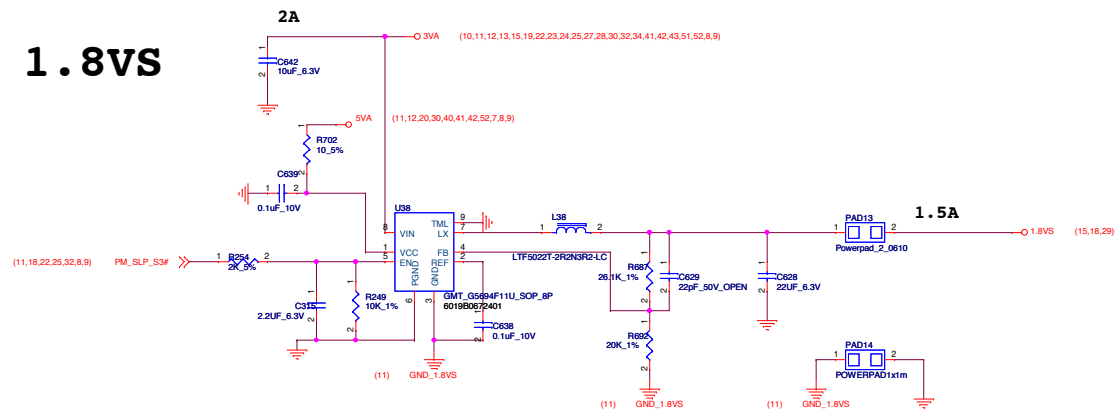
Strike

1.05VS/VCCP

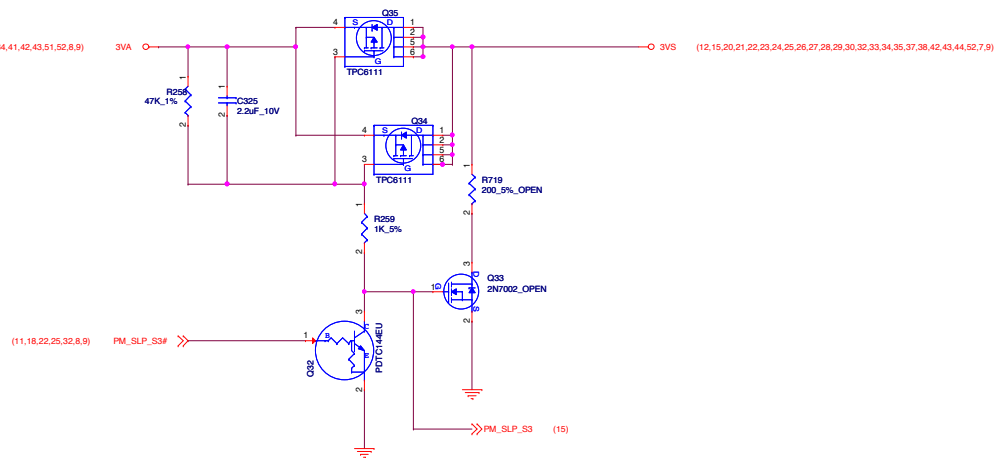
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	X01
SHEET	9	of	39



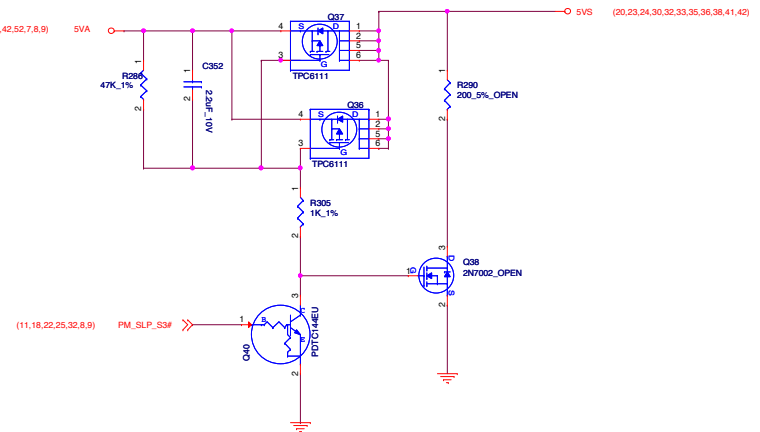
1.8VS



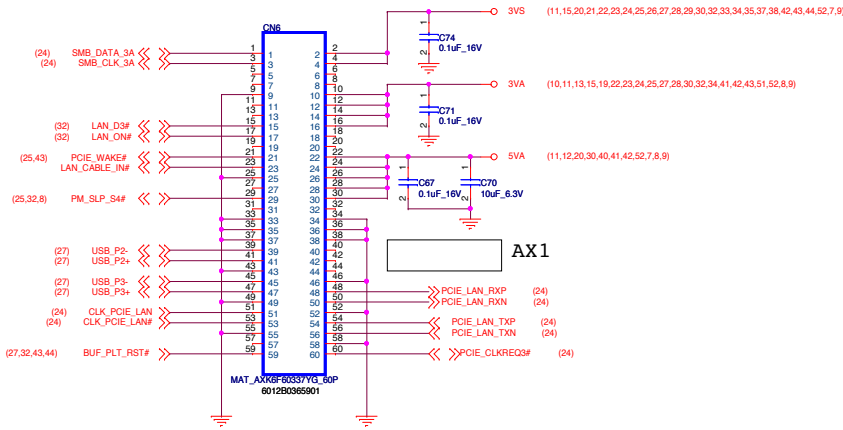
3VS



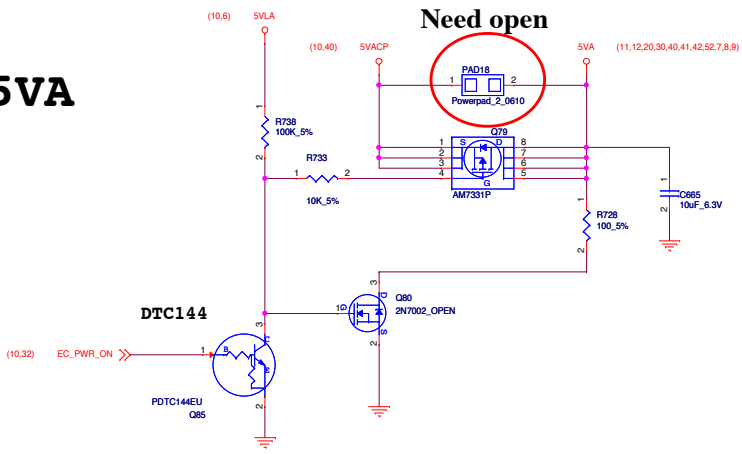
5VS



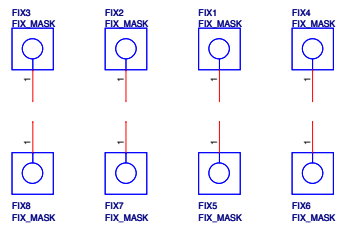
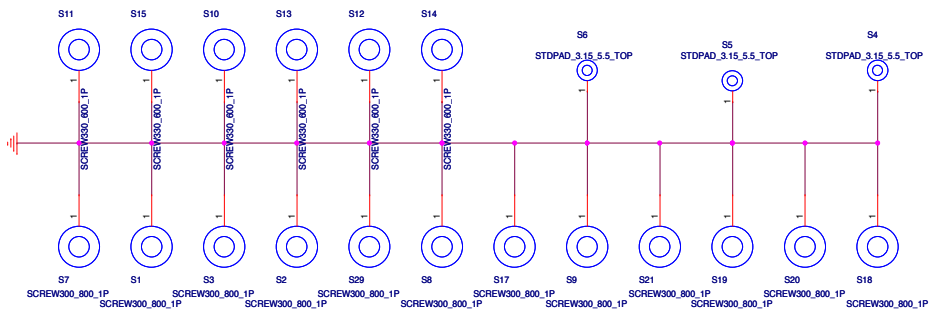
IO CNN



5VA

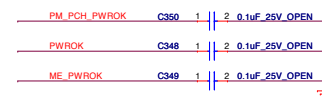
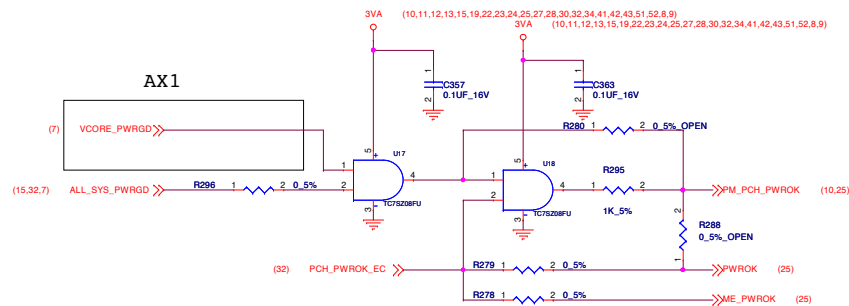
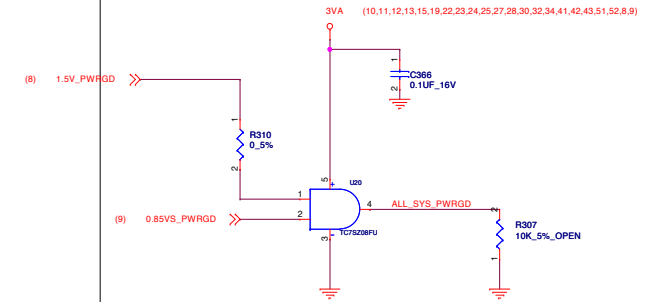


SCREW



## POWER SEQUENCE

AX1



(14,15,17,23,24,25,28,29,30,9) 1.05VS

R198

1 2

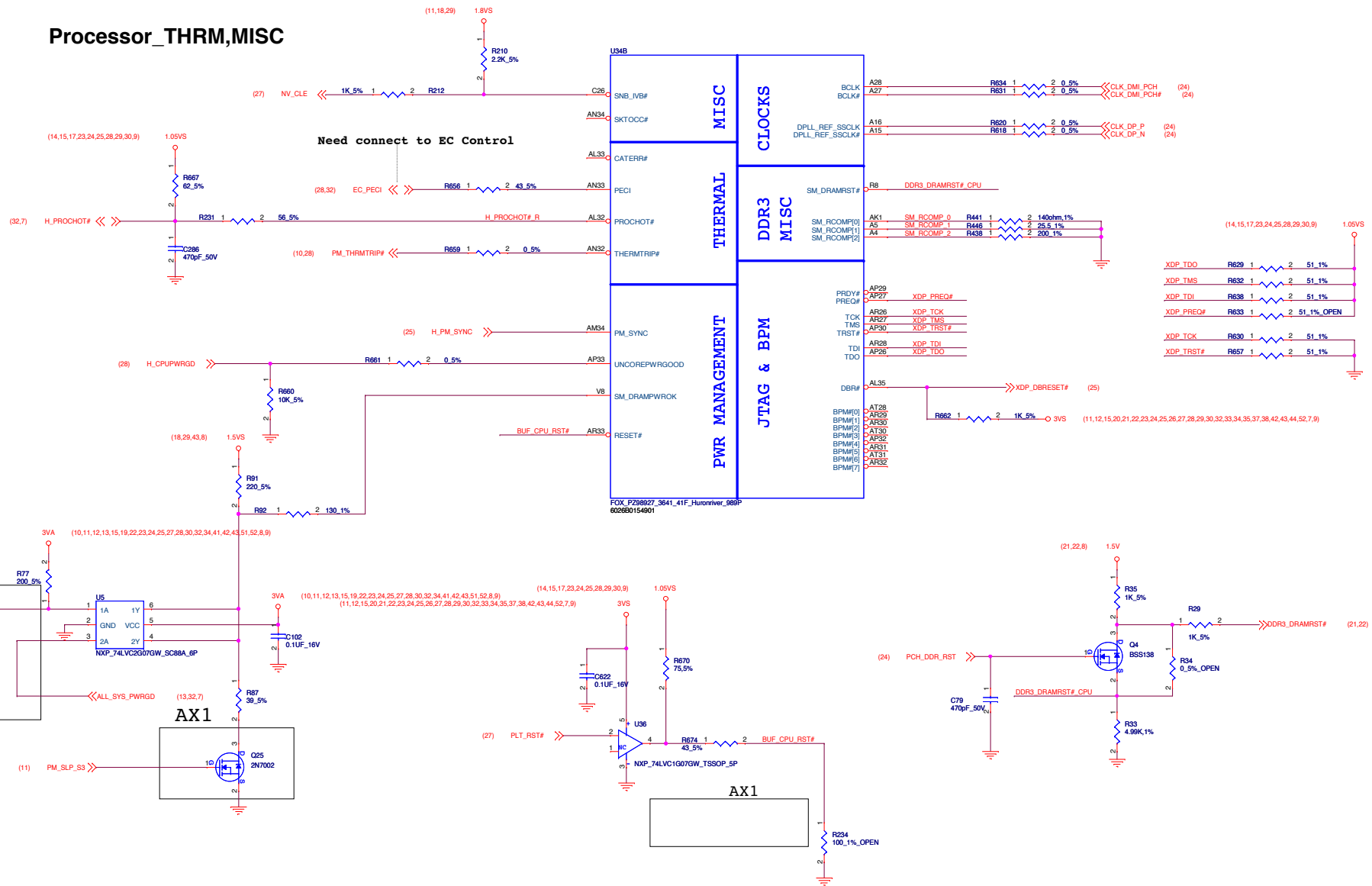
24.9\_1%



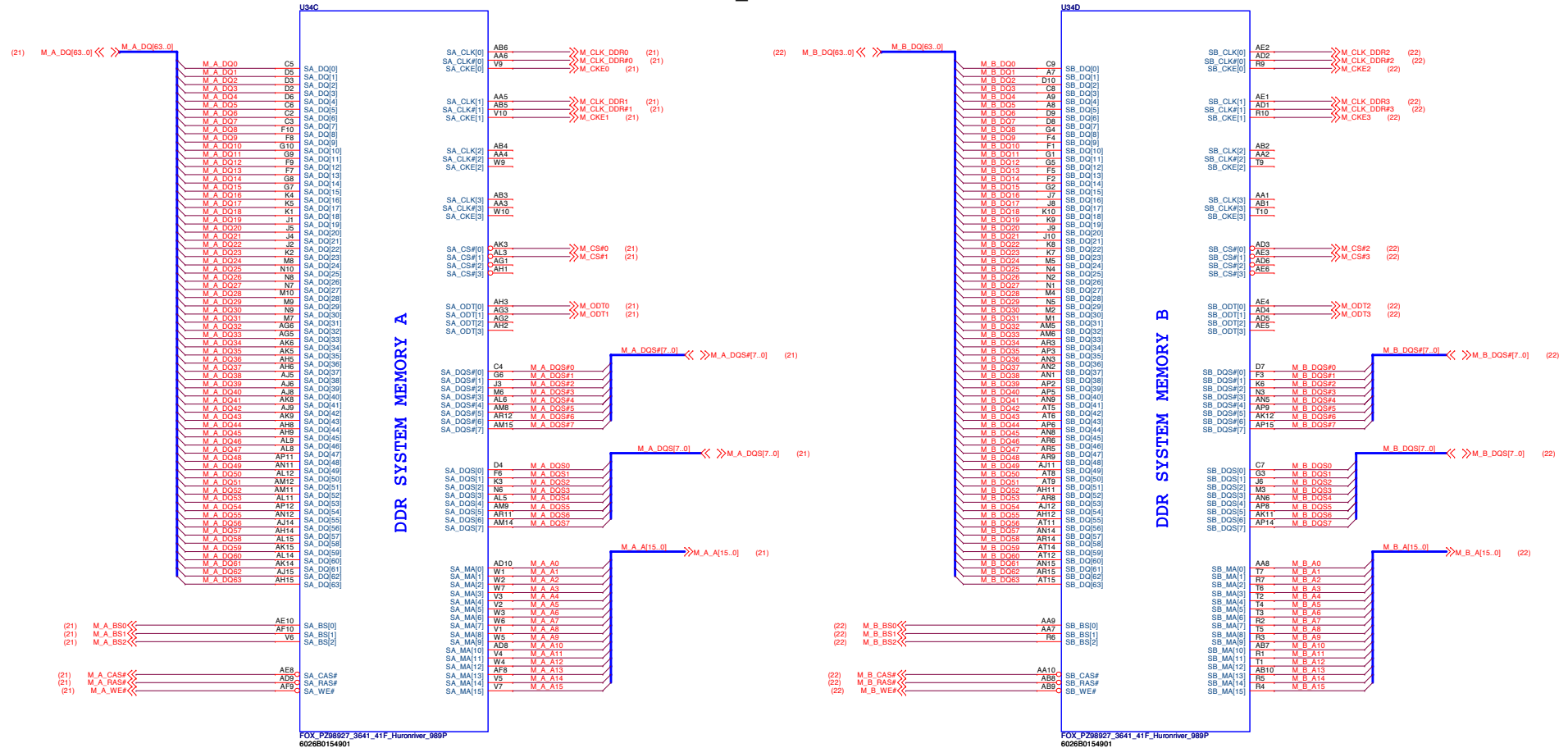
## CLOSED TO CPU

TITLE			
Strike Processor(1/6)			
SIZE B	CODE CS	DOC.NUMBER CS-131	REV X01
SHEET		14	of 59

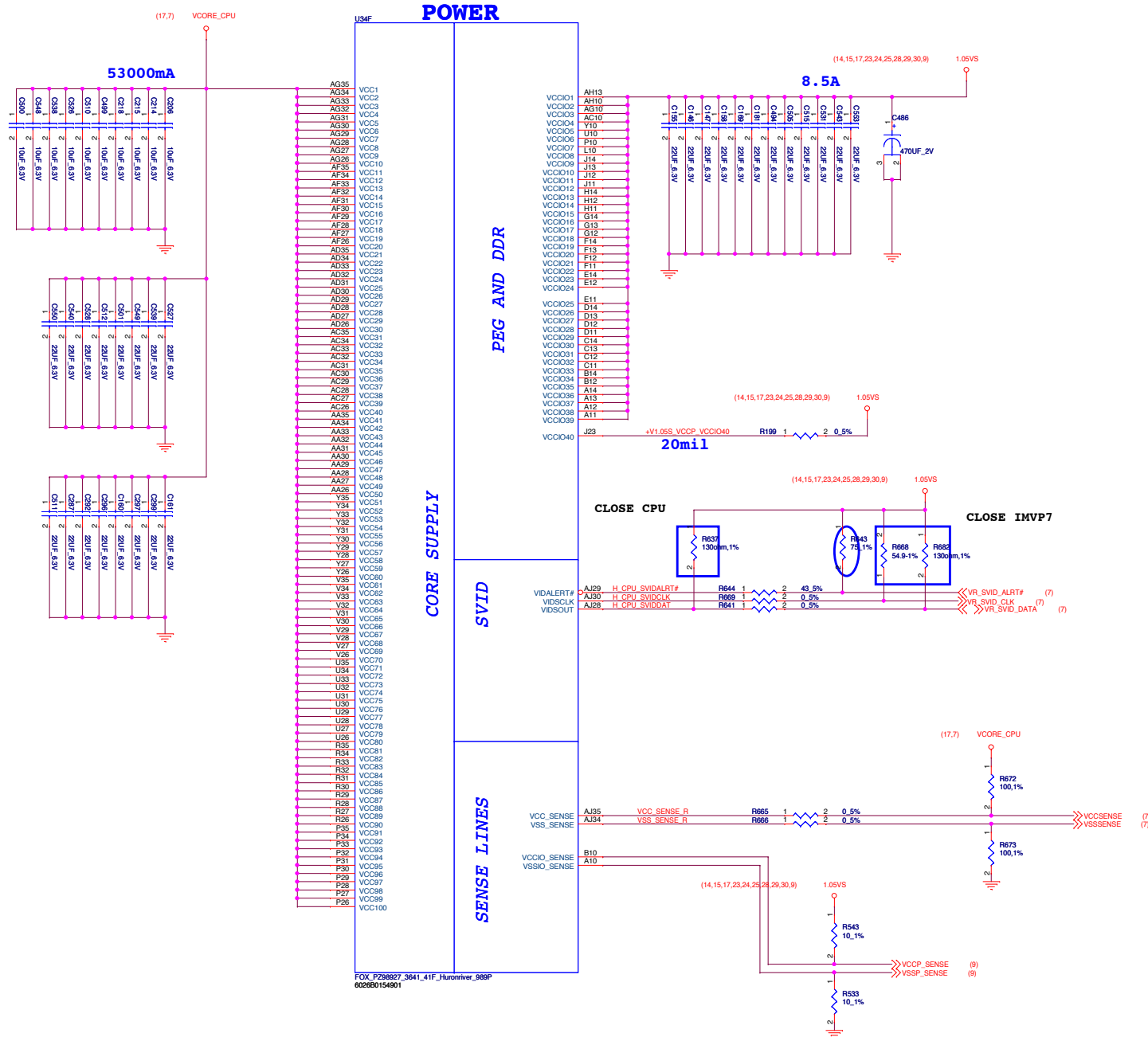
## Processor\_THRM,MISC



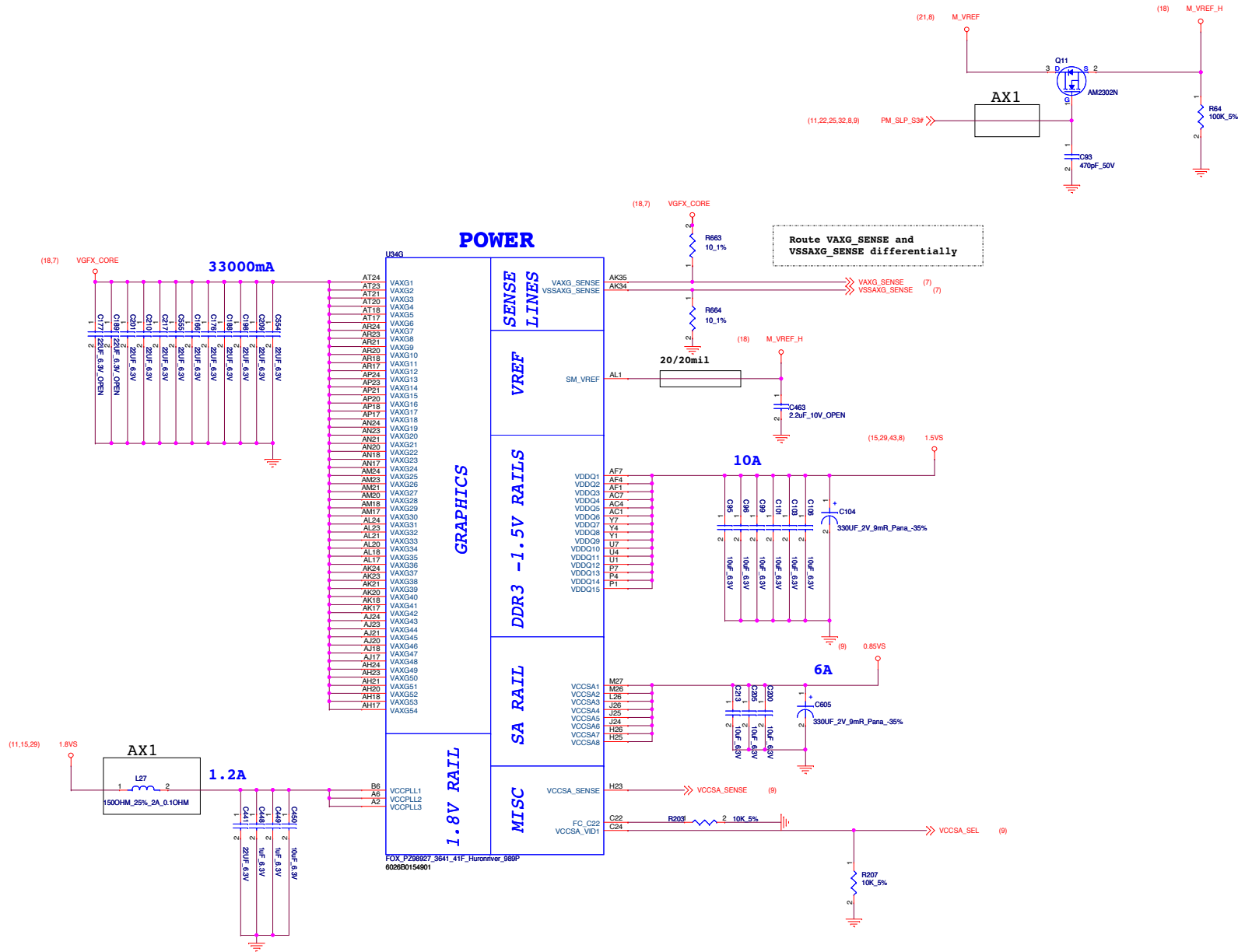
# Processor\_DDR3

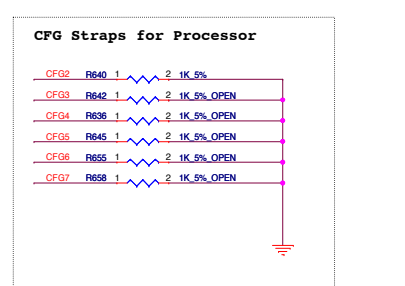
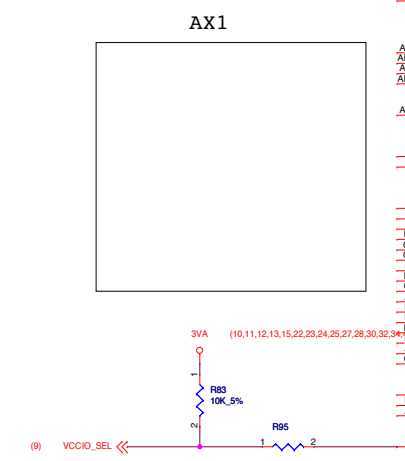
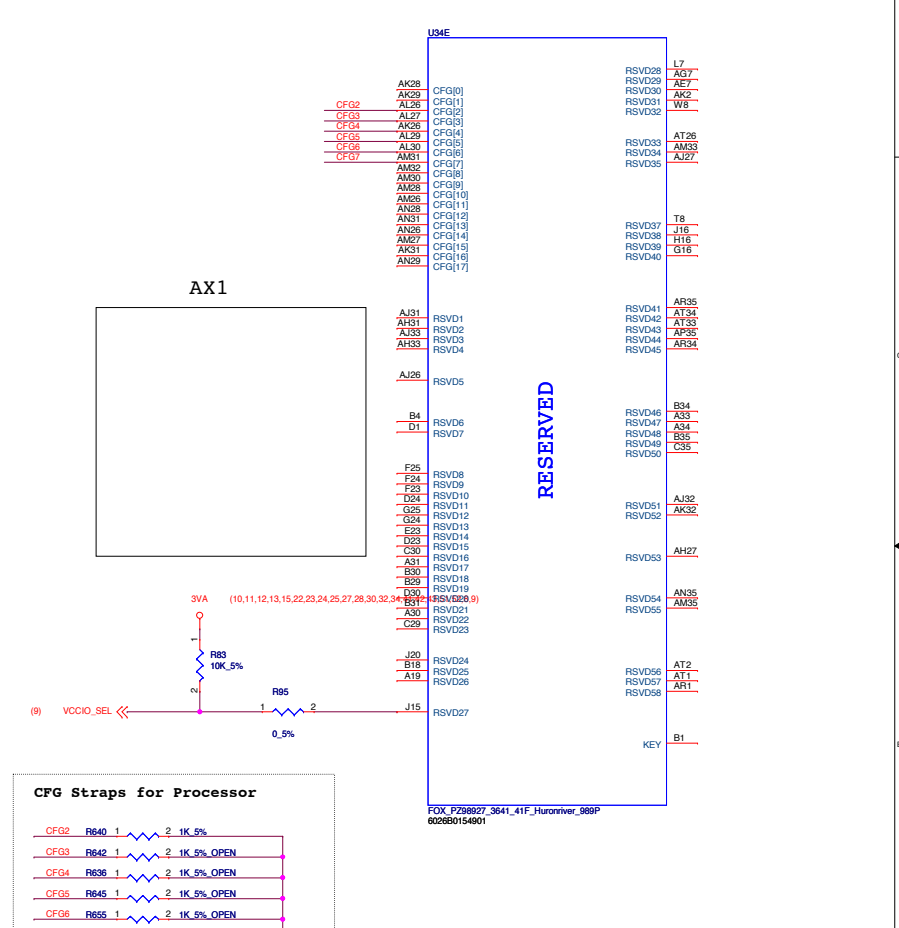
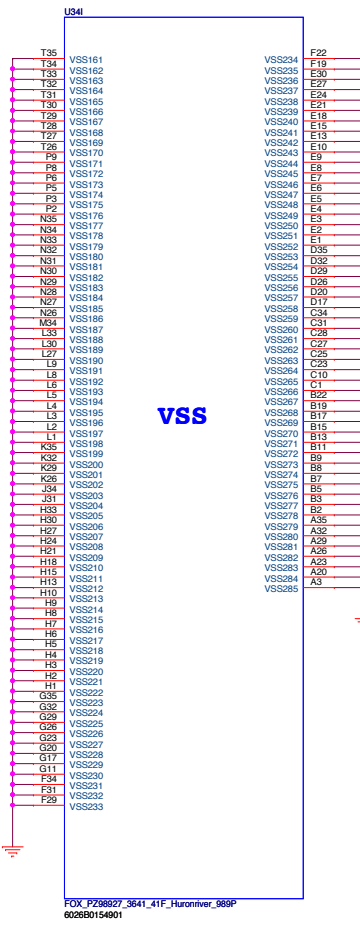
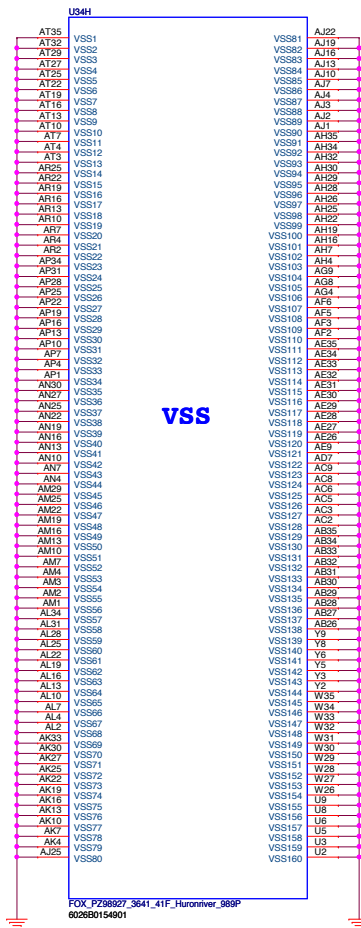






INVENTEC			
TITLE			
Strike Processor(4/6)			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01
SHEET		17	of 59



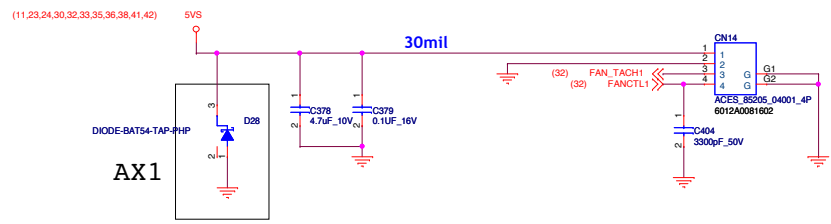


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Line # definition matches socket pin map definition 0:Lane Reversed
Display Port Presence Strap	
CFG2	1:(Default) Normal Operation; Line # definition matches socket pin map definition 0:Lane Reversed
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default)x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1:(Default) PEG Train immediately following RESETB de assertion 0:PEG Wait for BIOS for training

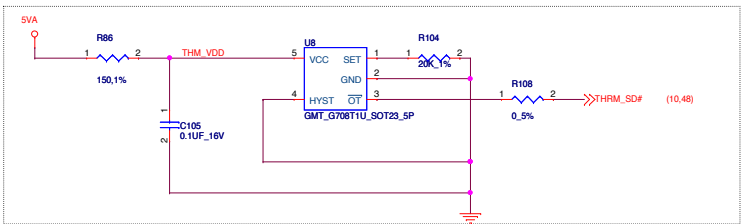
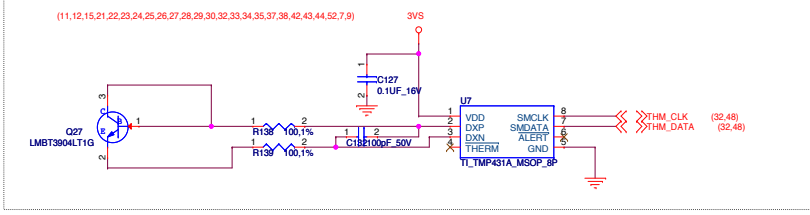
INVENTEC			
Strike Processor(6/6)			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01
SHEET		19	of 59

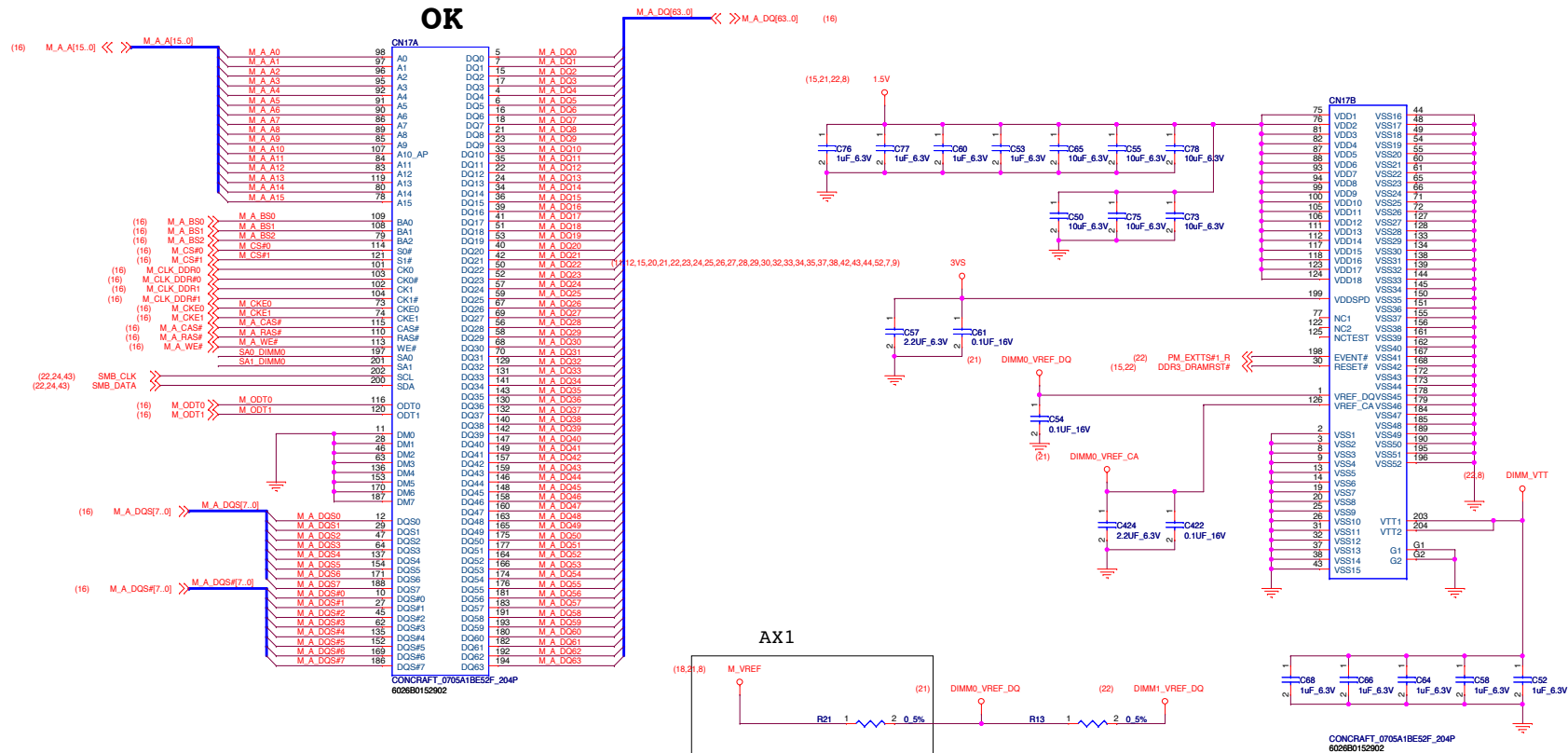
Fan control



GPU Thermal sensor

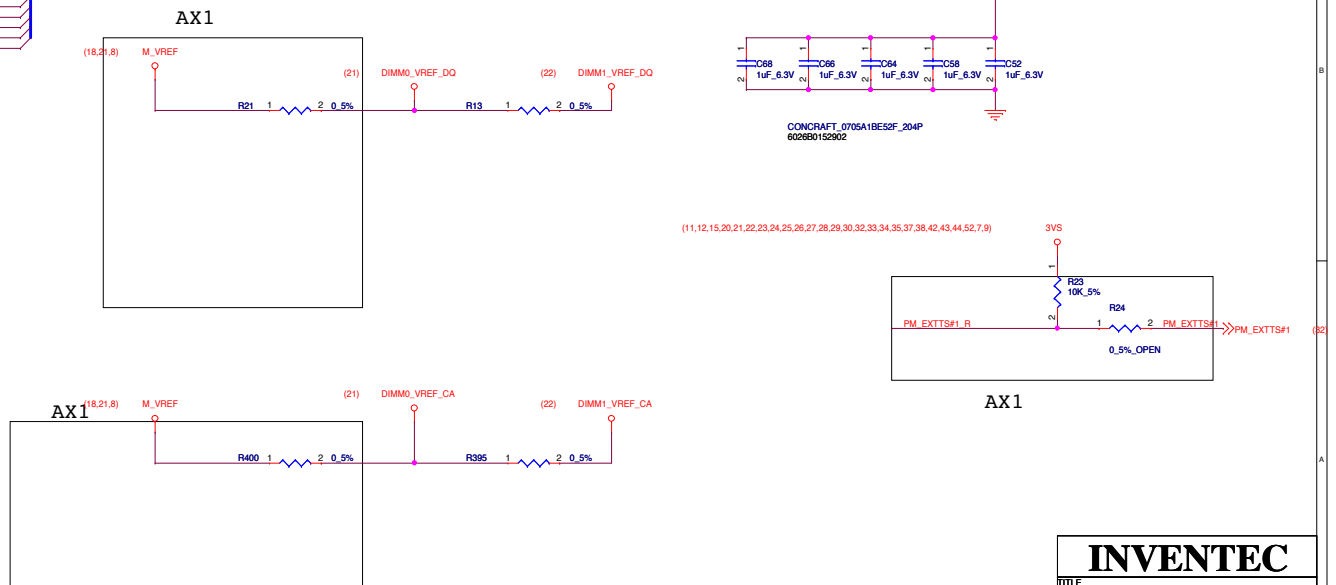
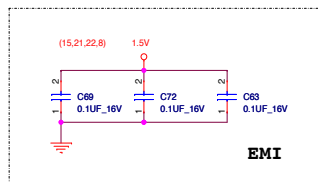
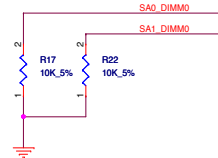
REMOTE thermal sensor  
Place near the hottest spot area under Palm-rest



**SO-DIMMO**

```
NOTE:
IF SAO DIMMO=0,SAI DIMMO=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30

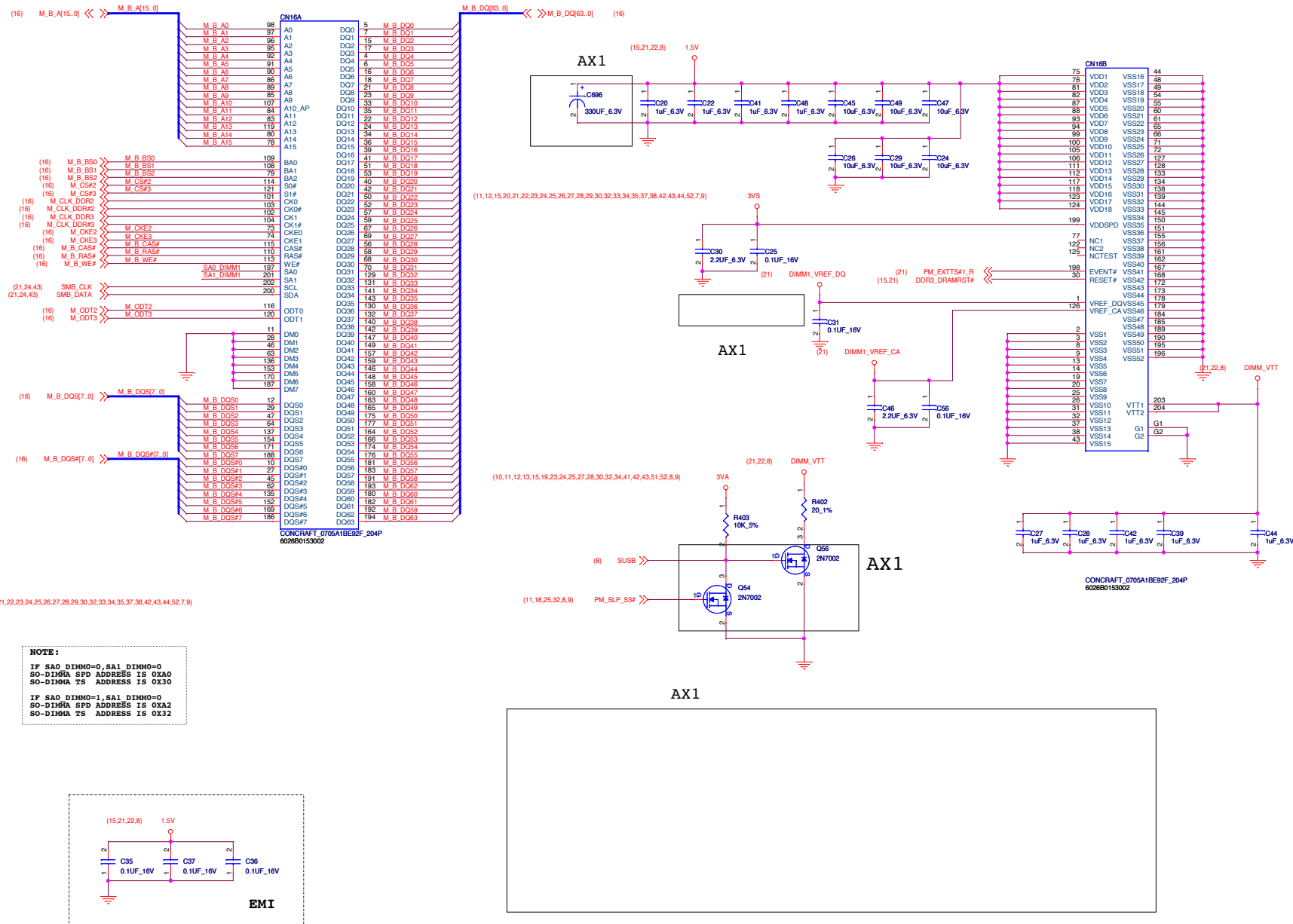
IF SAO DIMMO=1,SAI DIMMO=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32
```



<b>INVENTEC</b>			
TITLE			
<b>Strike</b> <b>DDR3 SDRAM SO-DIMM 1/2</b>			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01
SHEET		21 of	59

# SO-DIMM1

OK



**INVENTEC**

TITLE				
Strike				
DDR3 SDRAM SO-DIMM 2/2				
SIZE	CODE	DOC NUMBER	REV	
C	CS	CS-131	22	58
SHEET				

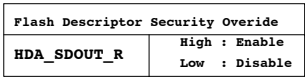
located on DIMM window area.

**CL1 CL2**

J1

JUMP2\_200\_32

3VA



TITLE			
Strike PCH(SATA,RTC,SPI)			
SIZE	CODE	DOC.NUMBER	REV
C	CS	CS-131	X01
SHEET		23	of 59

## WLAN

(43) PCIE\_WLAN\_RXN  
(43) PCIE\_WLAN\_RXP  
(43) PCIE\_WLAN\_TXN  
(43) PCIE\_WLAN\_TXP

## PCIE LAN

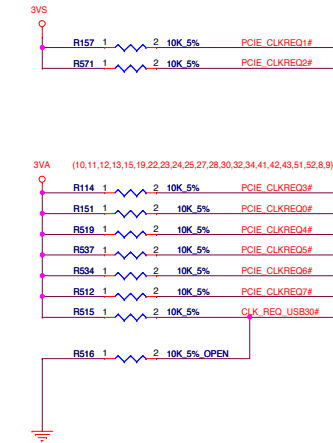
(12) PCIE\_LAN\_RXN  
(12) PCIE\_LAN\_RXP  
(12) PCIE\_LAN\_TXN  
(12) PCIE\_LAN\_TXP

## WLAN

(43) CLK\_PCIE\_WLAN#  
(43) CLK\_PCIE\_WLAN

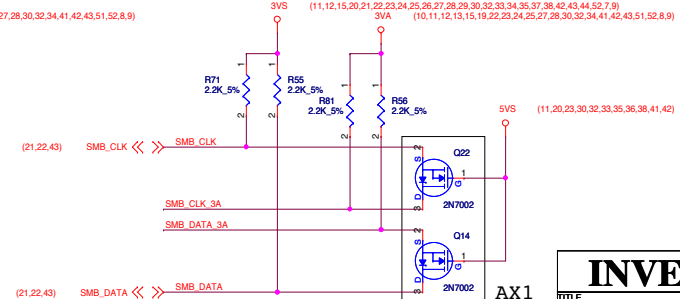
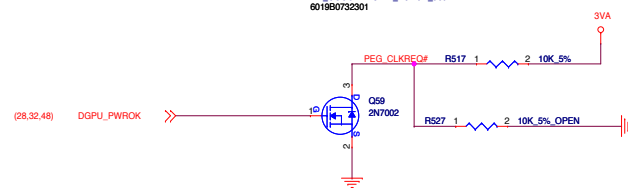
## LAN

(12) CLK\_PCIE\_LAN#  
(12) CLK\_PCIE\_LAN



PCIECLKREQ# 0,3,4,5,6,7 --- 3VA plane

PCIECLKREQ# 1,2 --- 3VS plane



# INVENTEC

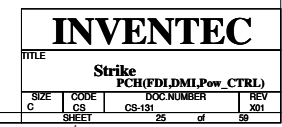
Strike  
PCH(PCL\_E, I2C)

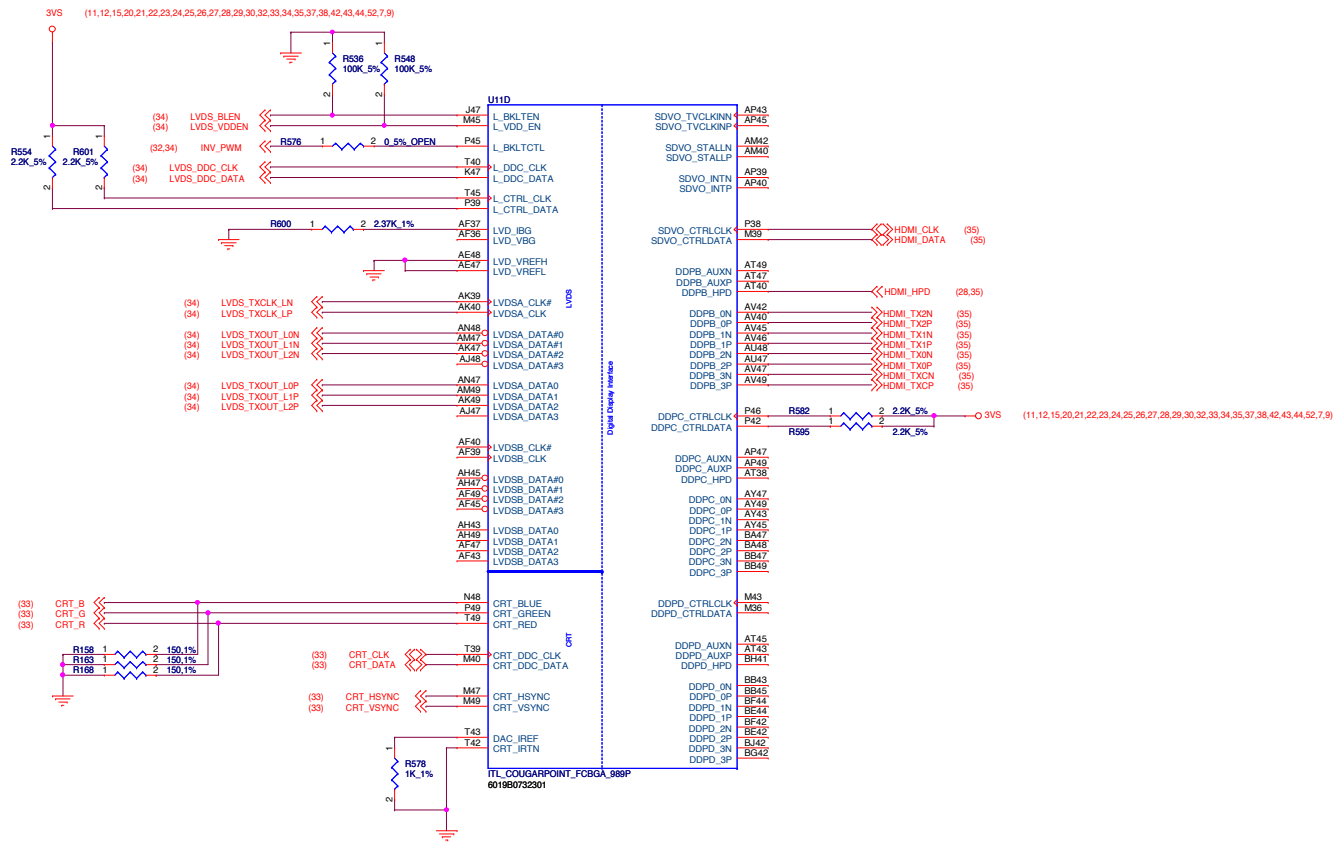
SIZE CODE DOC NUMBER  
C CS CS-131 24 of 59

CHANGE by IEC DATE Thursday, October 07, 2010

SHEET X01







Place 150ohm termination resistor close to GMCH

INVENTEC

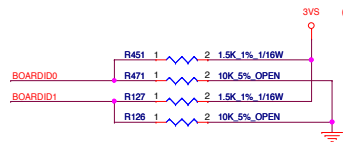
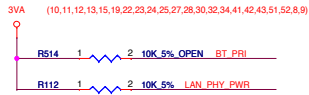
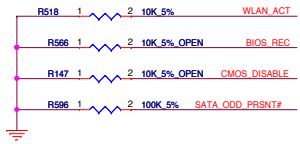
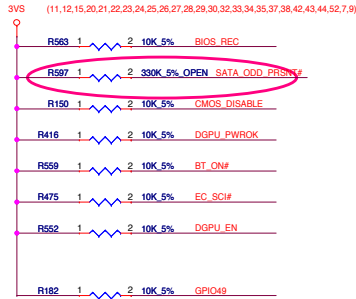
TITLE

Strike PCH(LVDS,CRT,HDMI)

SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01

SHEET 26 of 59

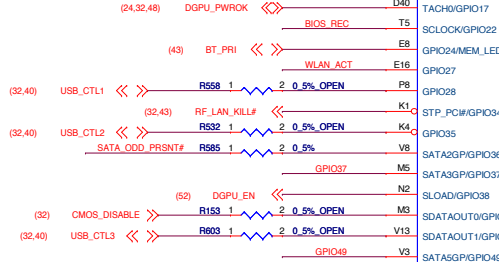




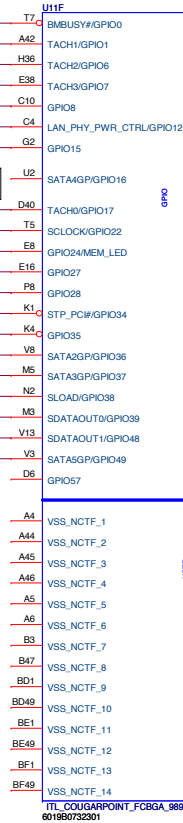
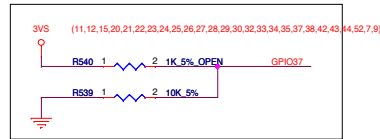
(11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52,7,9)

(10,11,12,13,15,19,22,23,24,25,27,28,30,32,34,41,42,43,51,52,8,9)

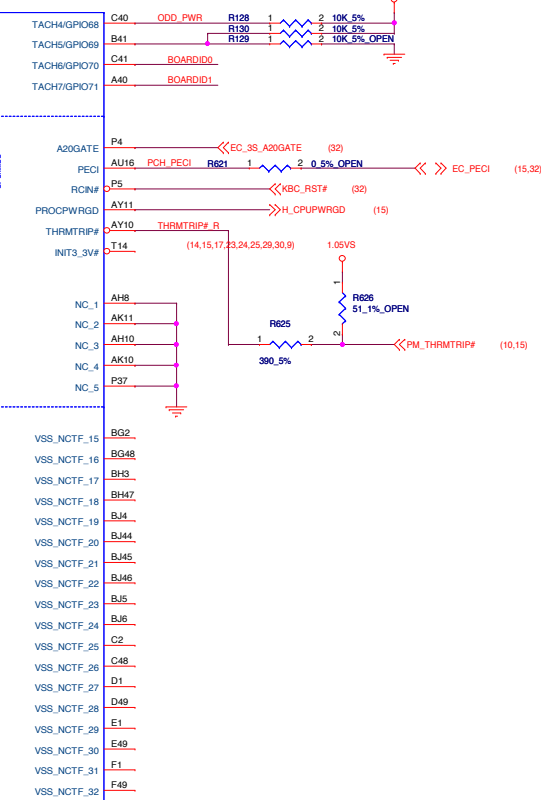
AX1



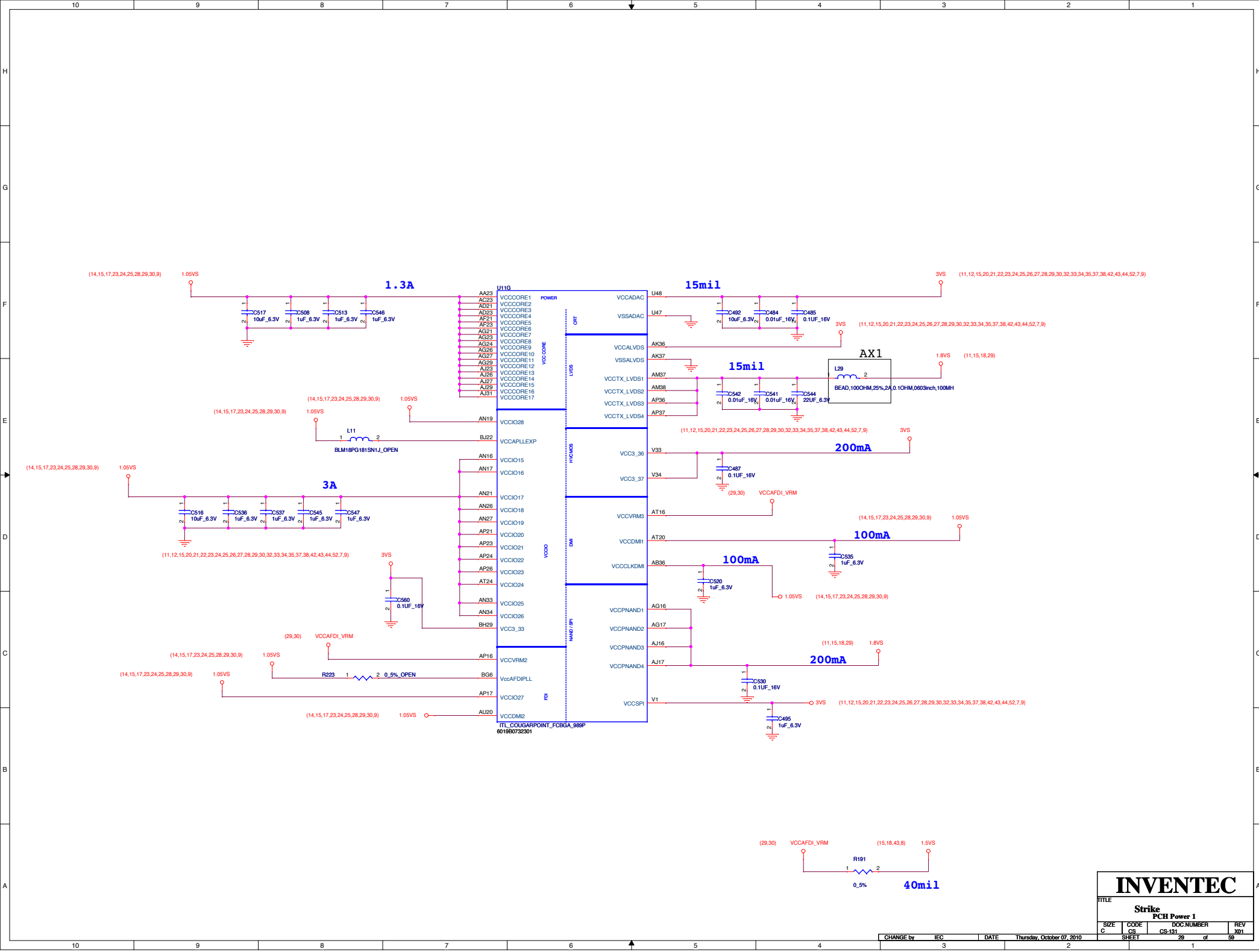
AX1



(11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52,7,9)

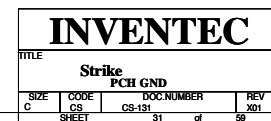


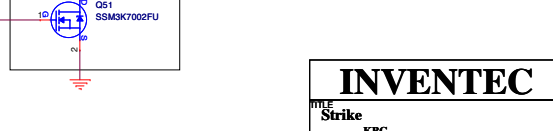
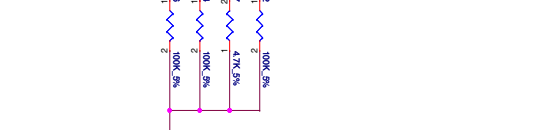
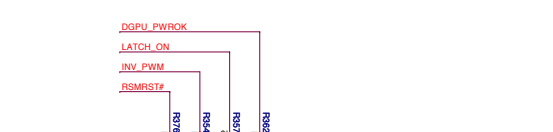
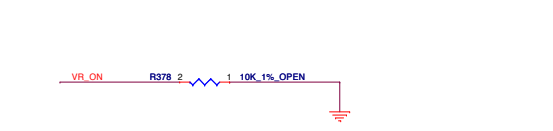
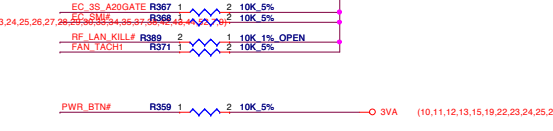
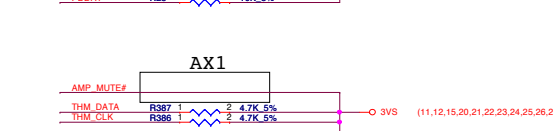
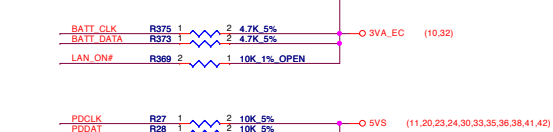
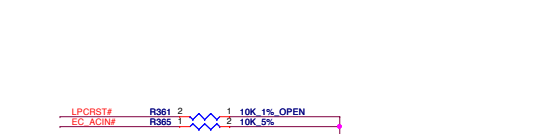
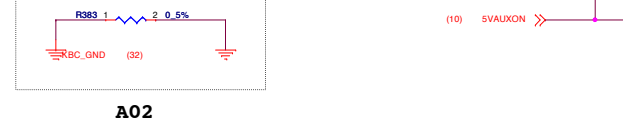
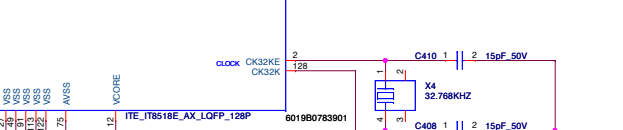
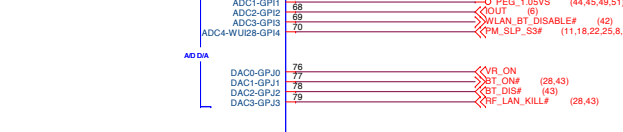
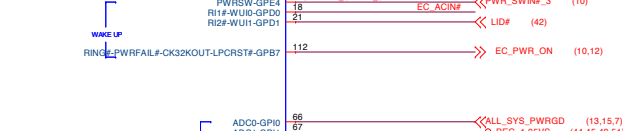
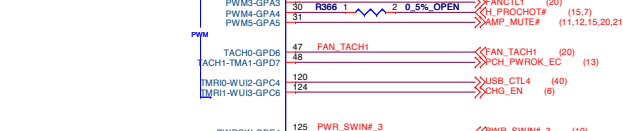
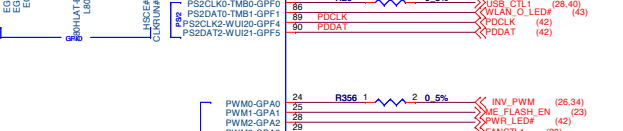
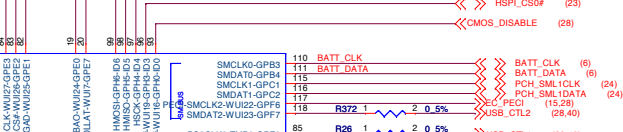
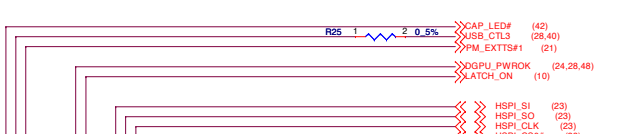
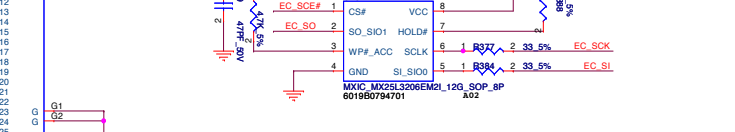
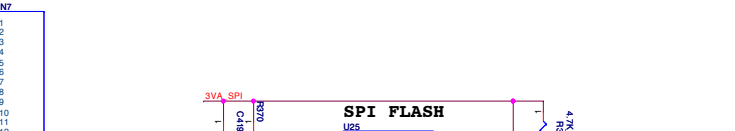
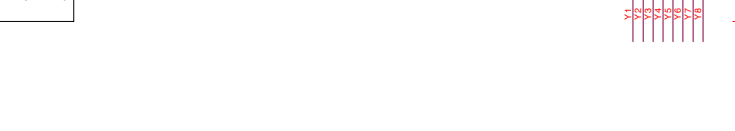
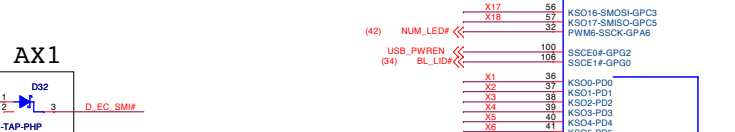
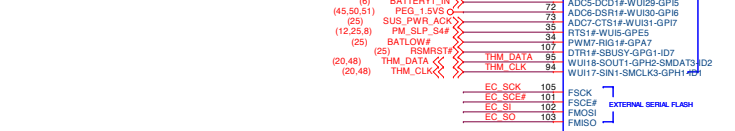
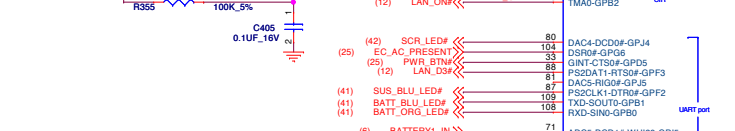
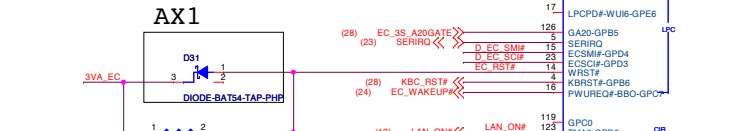
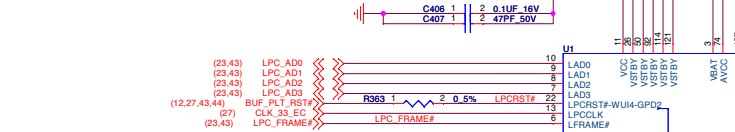
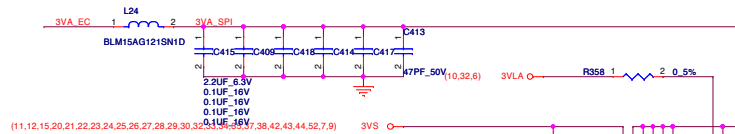
INVENTEC				
Strike FCH(MISC,GPIO)				
SIZE	CODE	DOC NUMBER	REV	
C	CS	CS-131	X01	
SHEET		28	of 59	



INVENTEC			
TITLE			
Strike PCH Power 1			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01
SHEET		29	of 59







A02

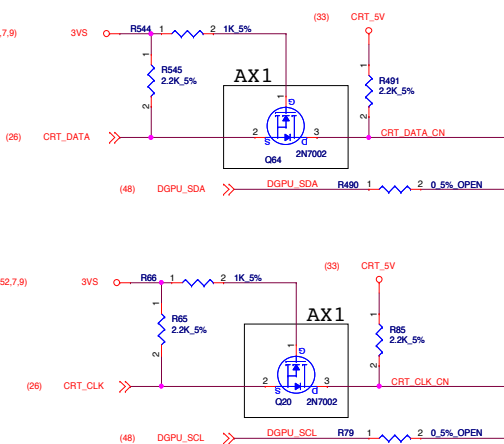
<b>INVENTEC</b>			
MIL-STD-883C			
KBC			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	X01
CHANGE by		DATE	Thursday, October 07, 2010
SHEET		32	of 39



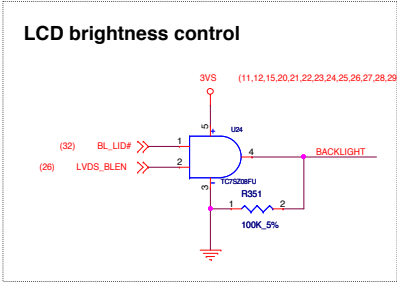
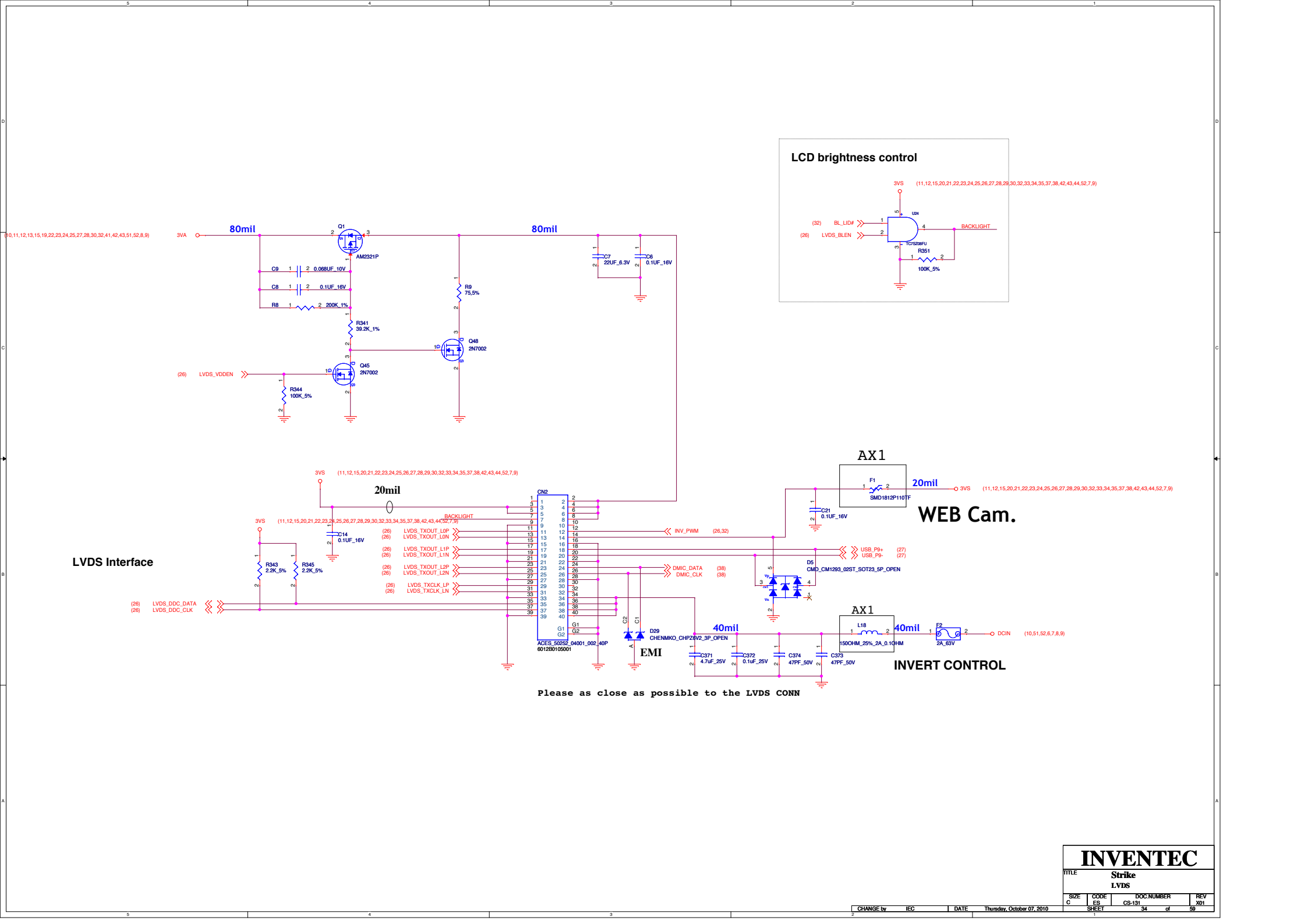
(11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52,7,9)



20mil



CHANGE by IEC		DATE Thursday, October 07, 2010	C	CS	CS-131	X01
			SHEET 33 of 59			

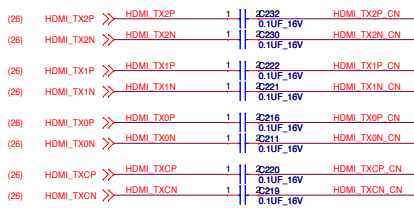
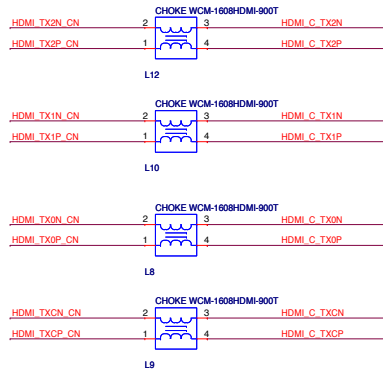


**LVDS Interface**

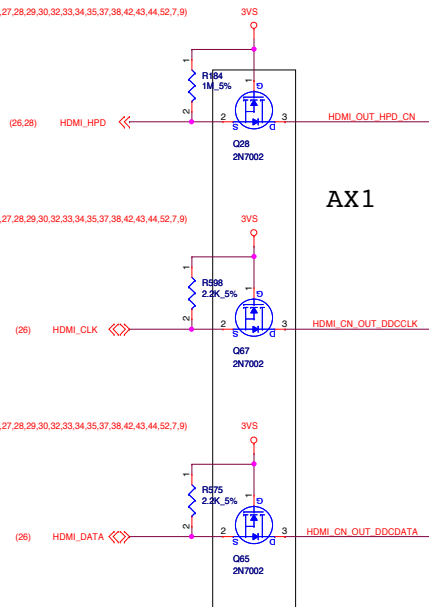
**WEB Cam.**

**INVERT CONTROL**

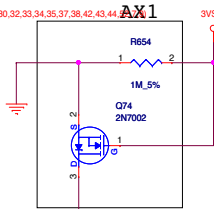
Please as close as possible to the LVDS CONN



(11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52,7,9)

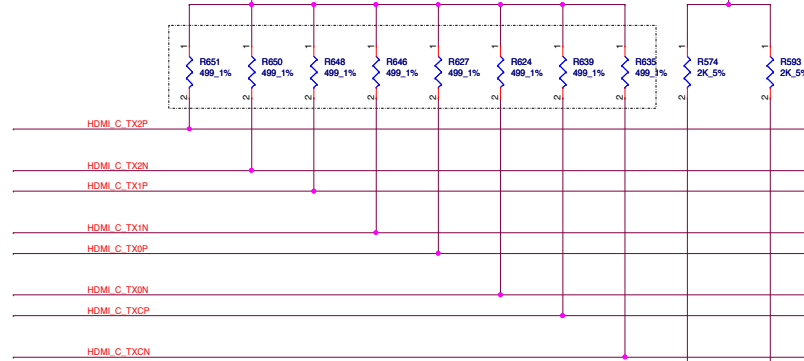
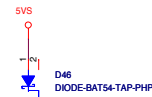


(11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44)



## HDMI CONN

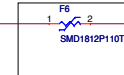
(11,20,23,24,30,32,33,35,36,38,41,42)



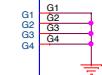
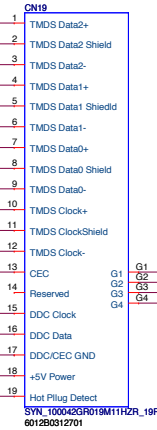
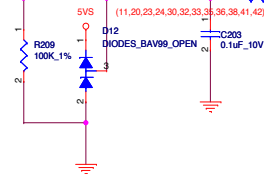
(11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52,7,9)

AX1

(11,20,23,24,30,32,33,35,36,38,41,42)



HDMI\_CN\_OUT\_DDCCLK  
HDMI\_CN\_OUT\_DDCDATA

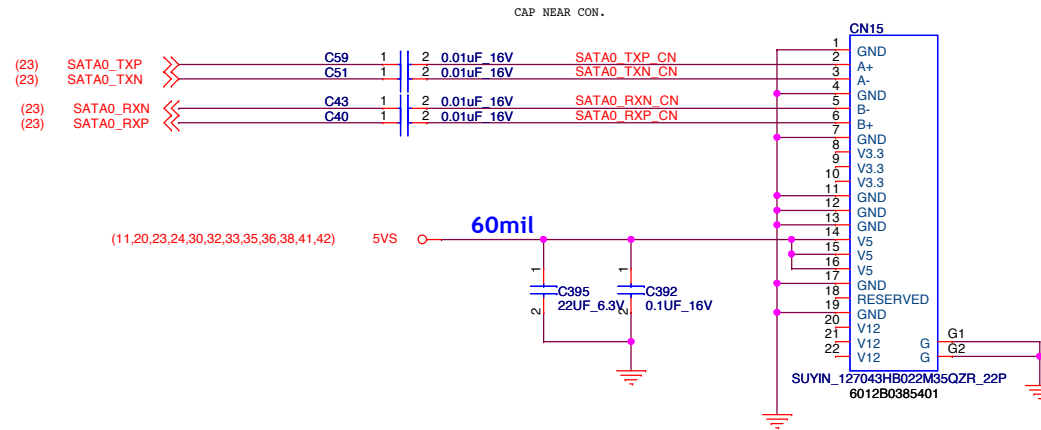


SYN\_100042GR019M1THZR\_19P  
601290312701

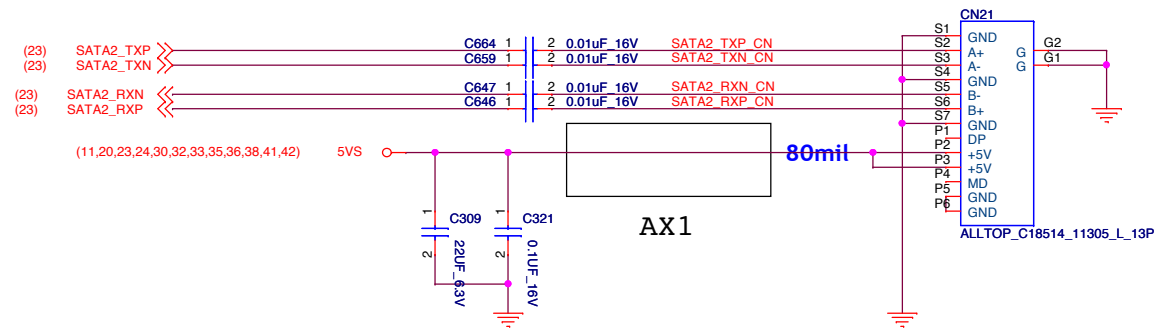
## INVENTEC

TITLE			
Strike HDMI CNN			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01
SHEET		35 of 59	

# HDD I/F



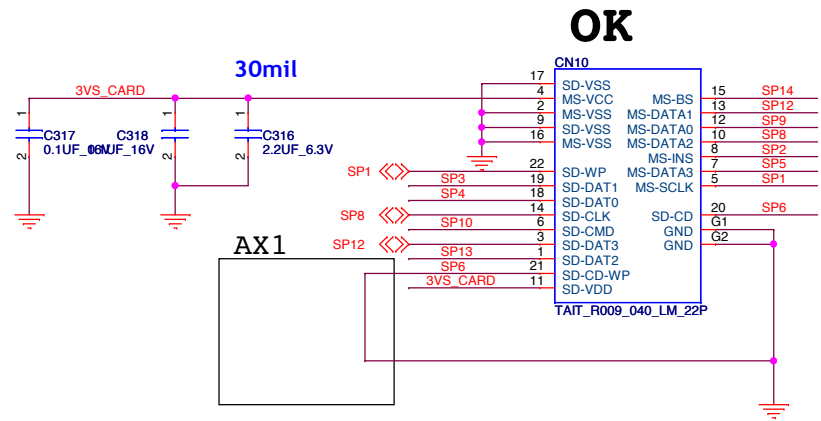
# ODD I/F



## INVENTEC

TITLE			
Strike HDD/ODD			
SIZE	CODE	DOC.NUMBER	REV
B	CS	CS-131	X01
SHEET		36 of 59	

CHANGE by IEC DATE Thursday, October 07, 2010

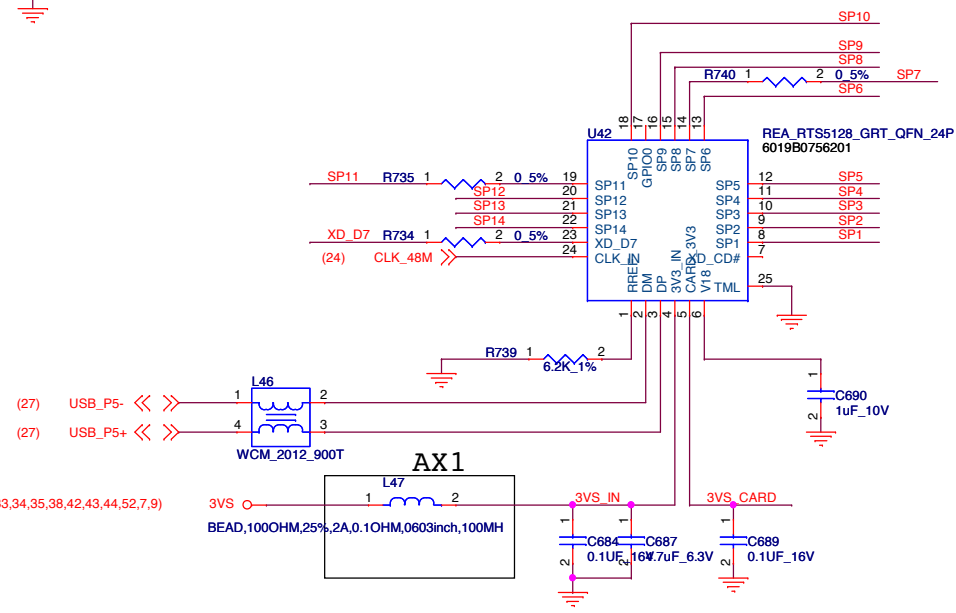


OK

AX1

CN10

TAIT\_R009\_040\_LM\_22P

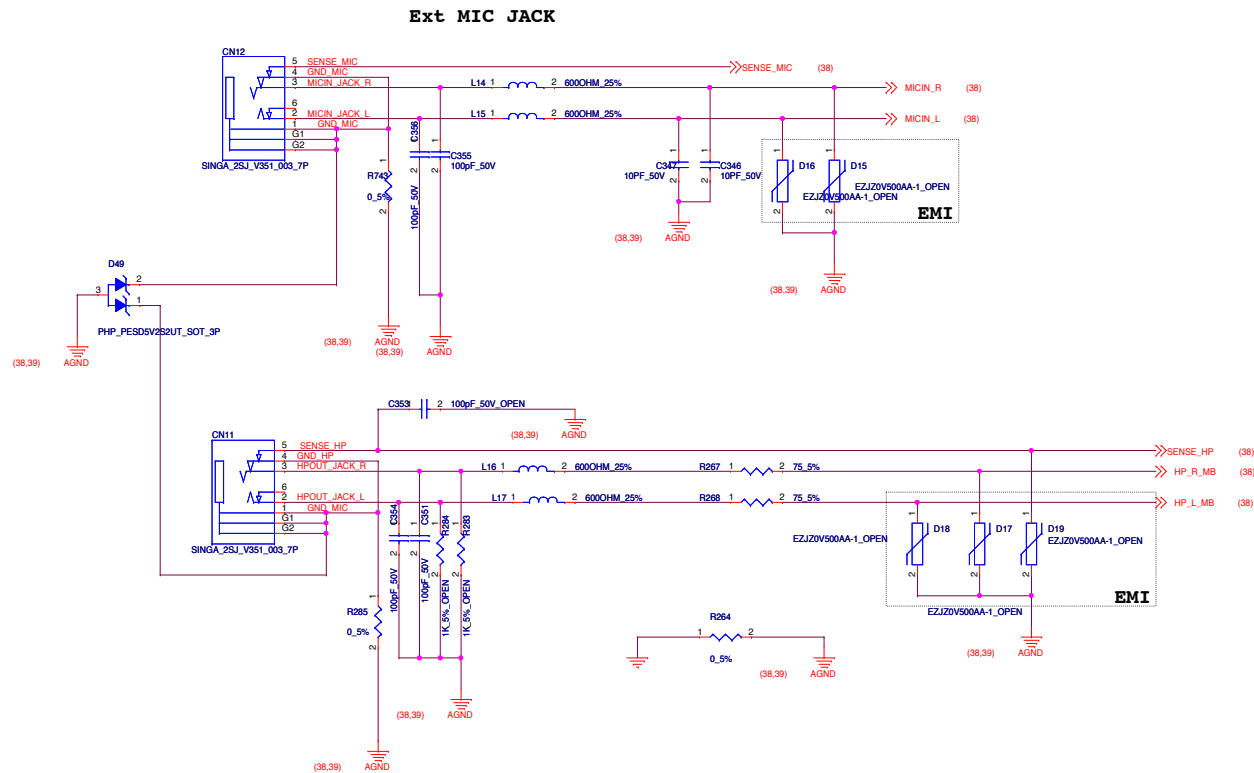


AX1

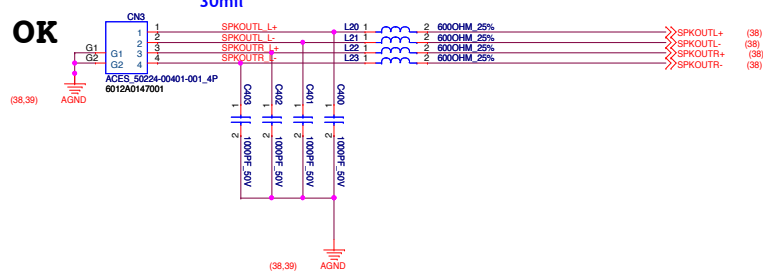
INVENTEC			
TITLE			
Strike Card reader			
SIZE	CODE	DOC.NUMBER	REV
B	CS	CS-131	X01
SHEET		37	of 59

CHANGE by IEC DATE Thursday, October 07, 2010





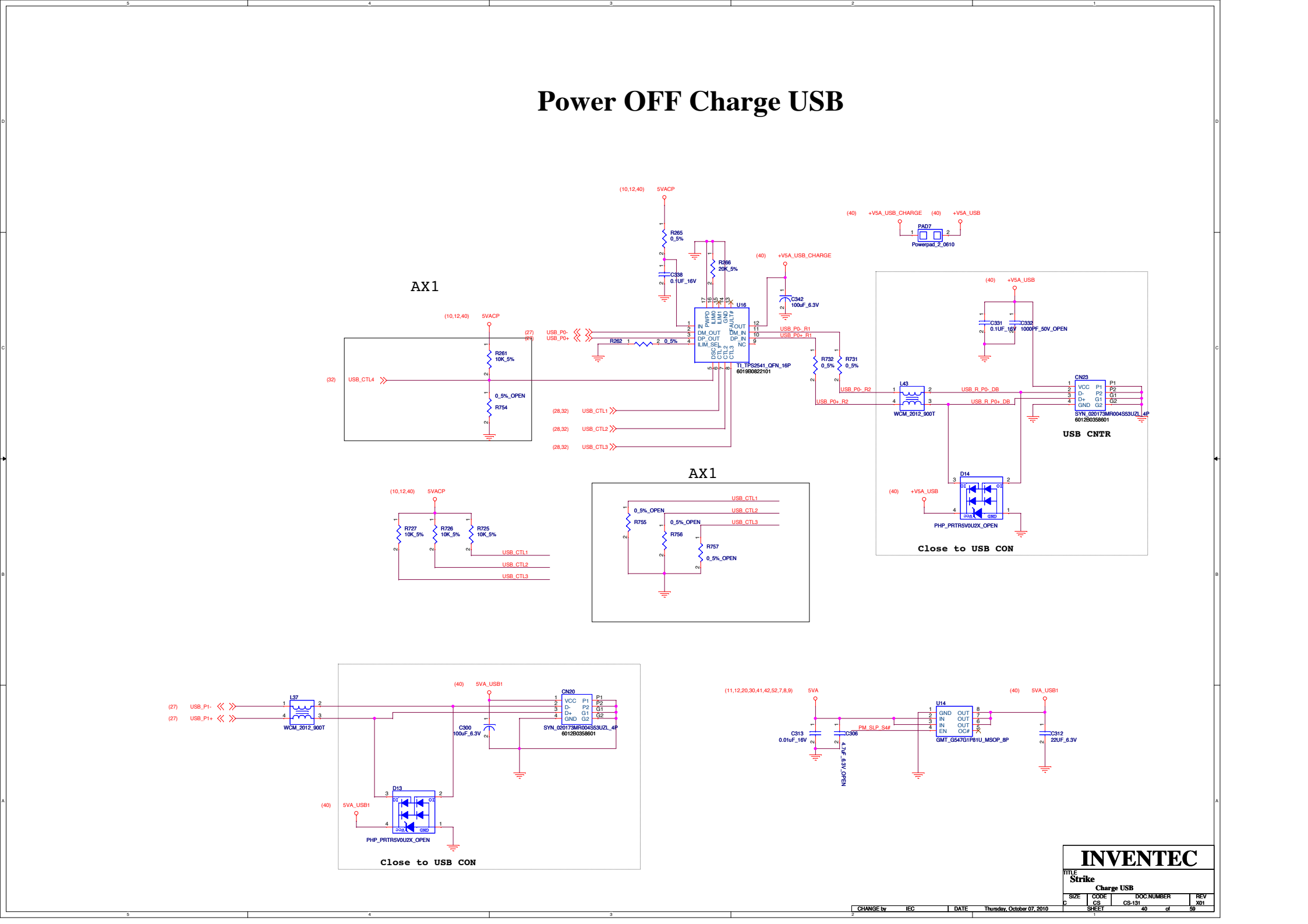
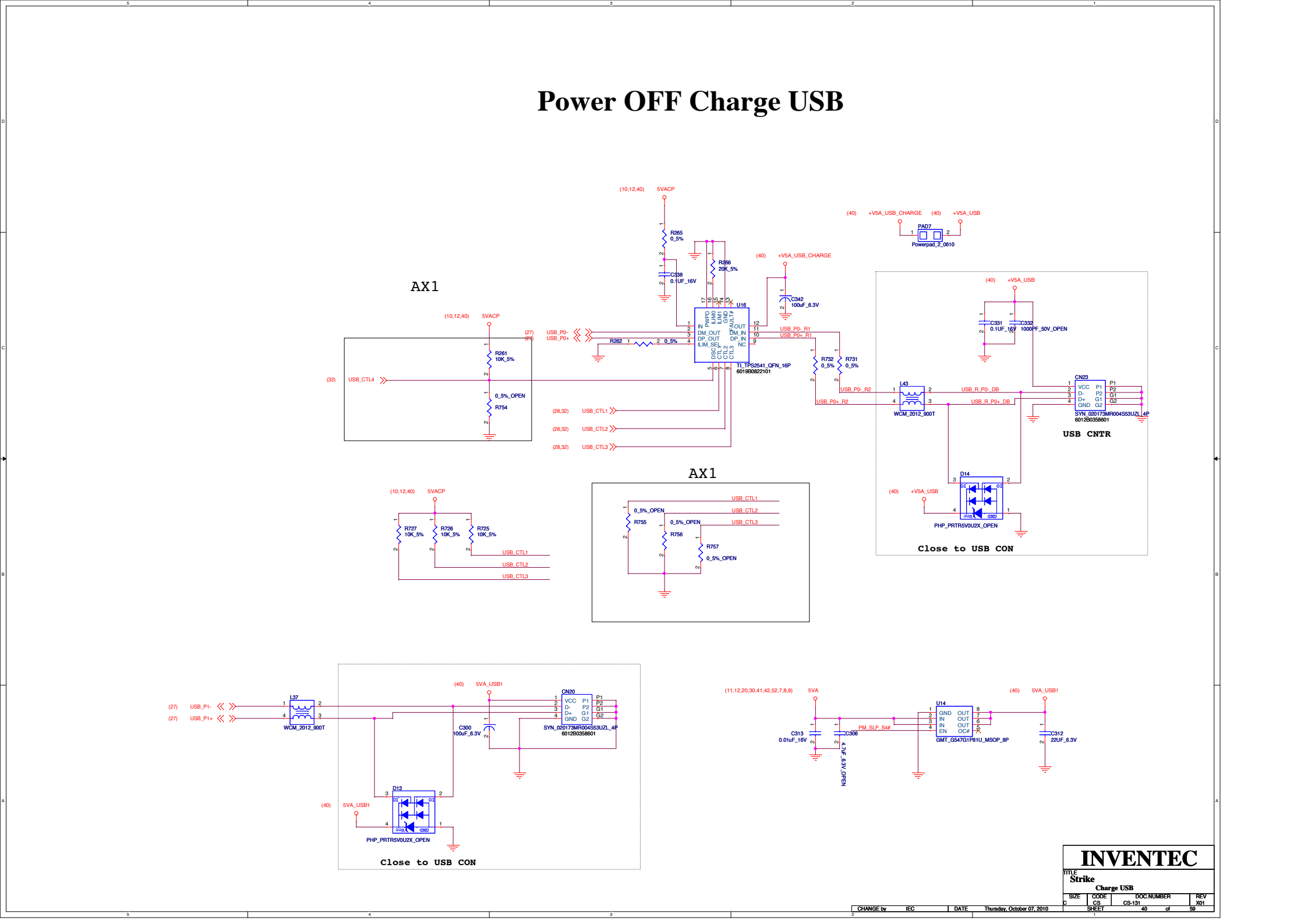
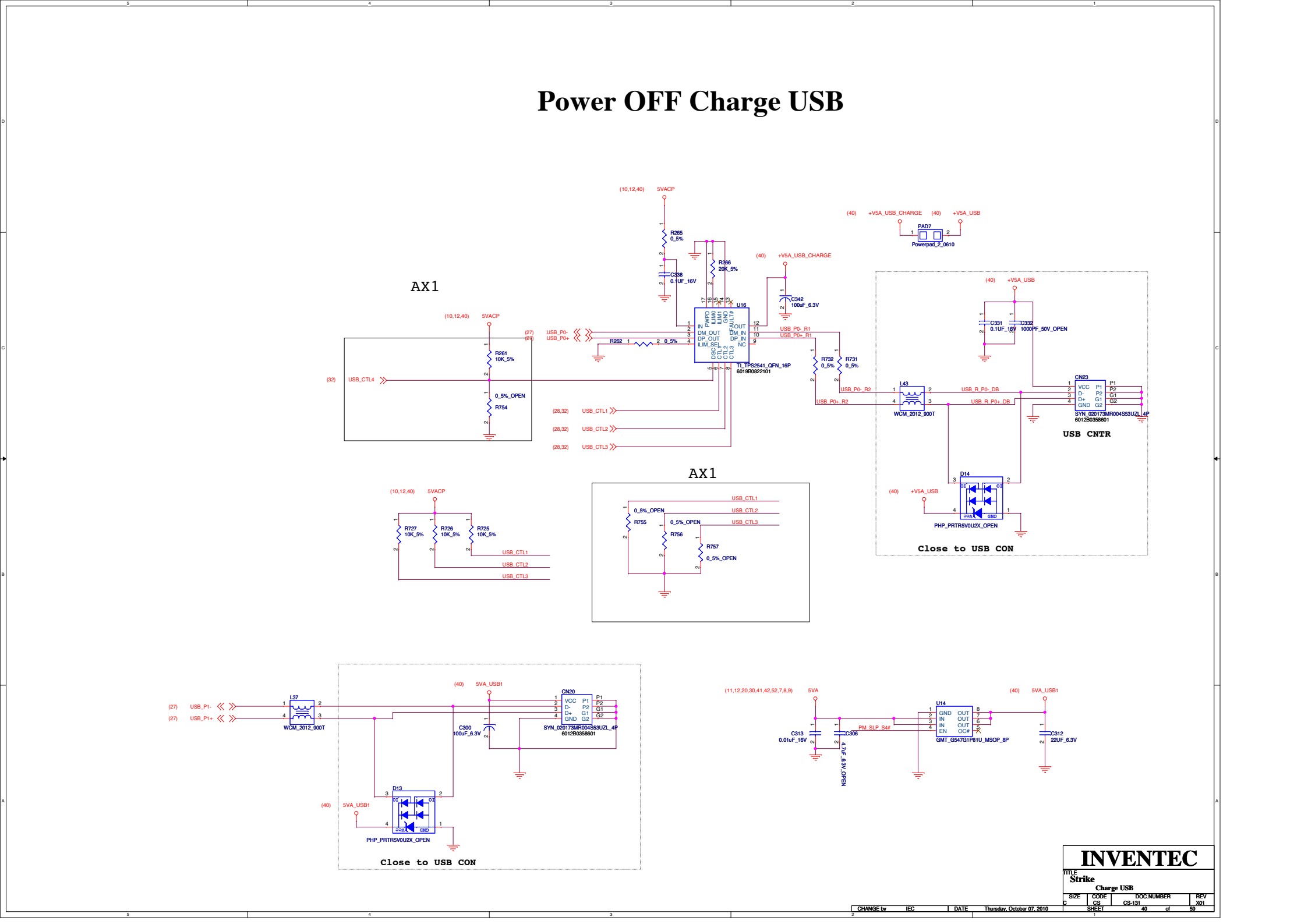
**OK**



**INVENTEC**

TITLE			
Strike			
Audio			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01
SHEET		39	of 59

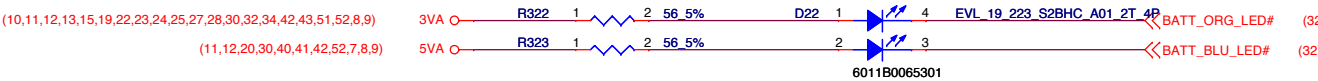
# Power OFF Charge USB







BLUE

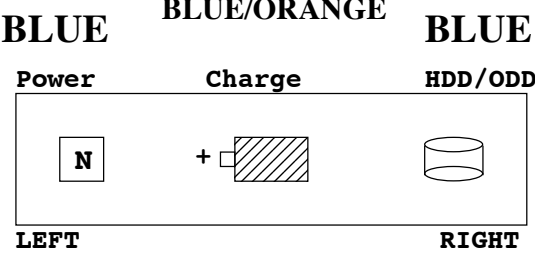


BLUE/ORANGE



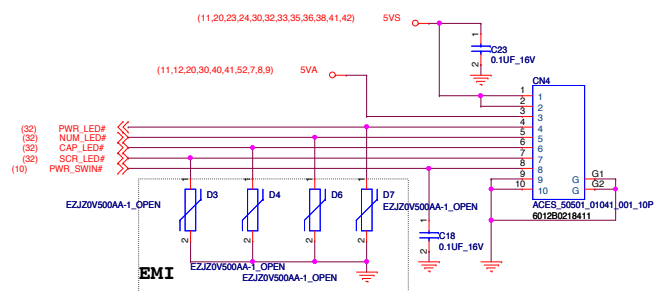
BLUE

LED Seat

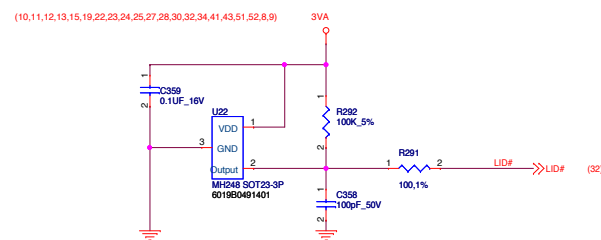


INVENTEC			
TITLE Strike LED			
SIZE B	CODE CS	DOC.NUMBER CS-131	REV X01
SHEET 1 41 of 59			

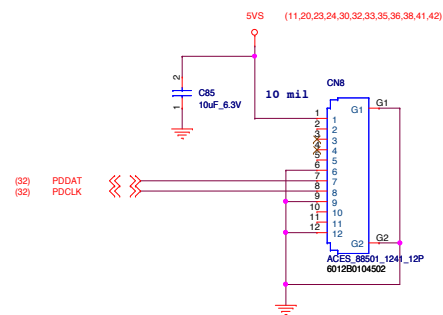
## EMI POWER BUTTON BOARD



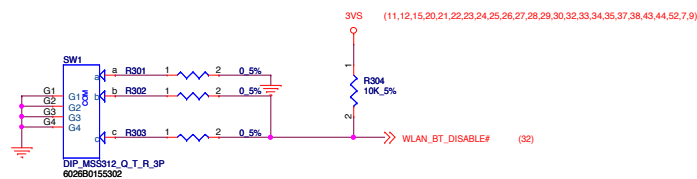
## HALL Switch



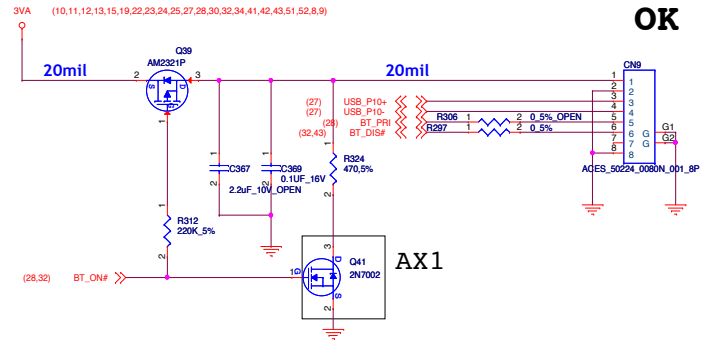
## GP CNN.



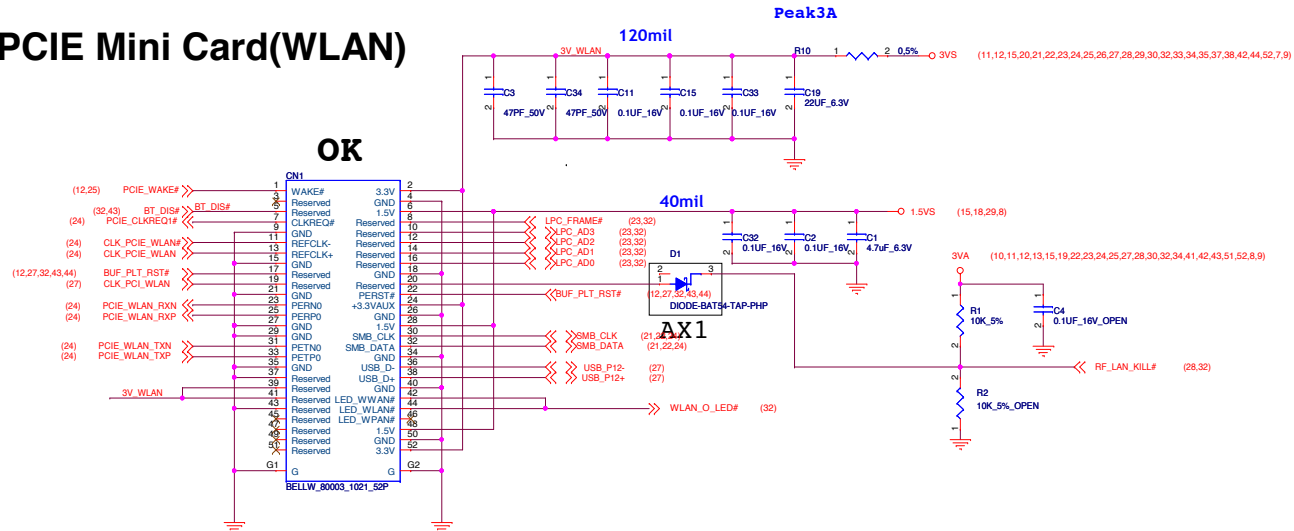
**(W-LAN, BT) sliding switch**



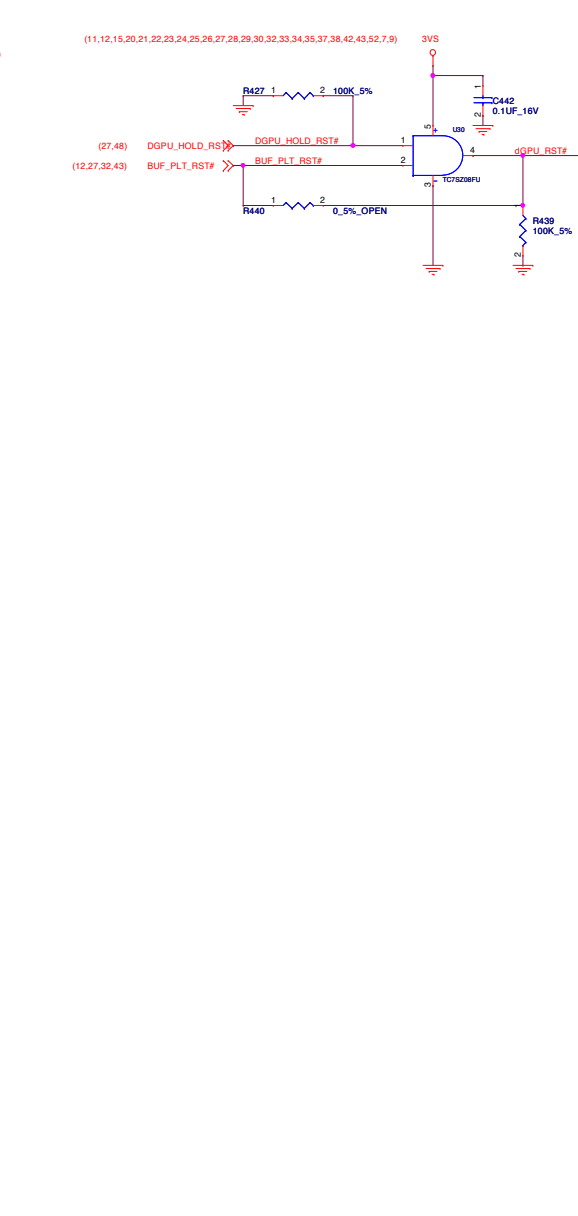
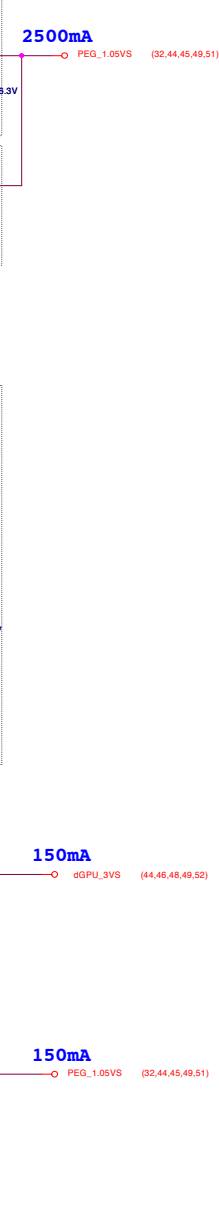
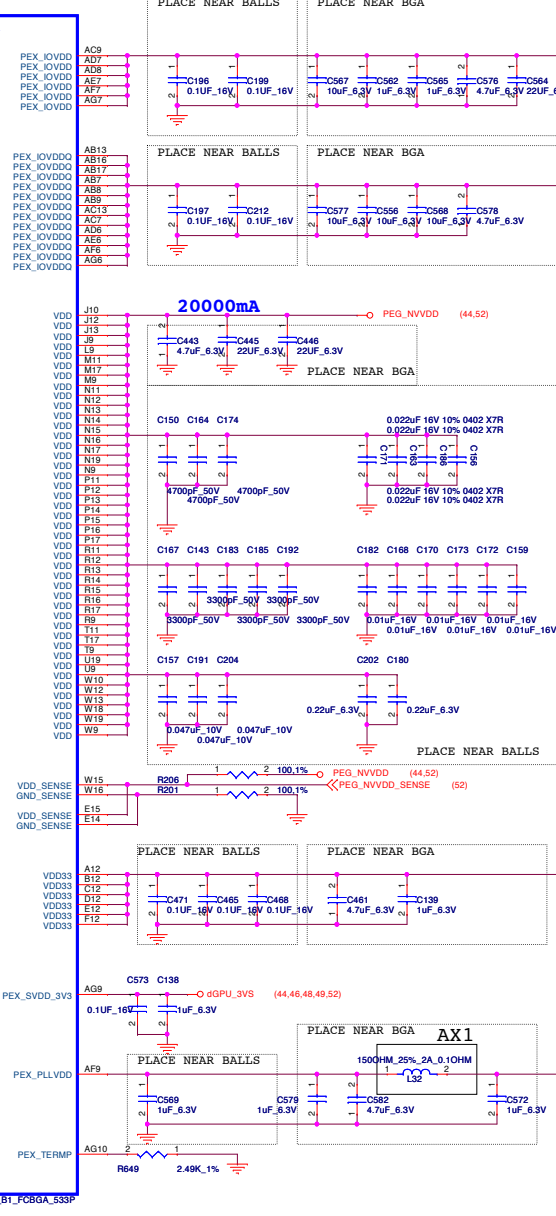
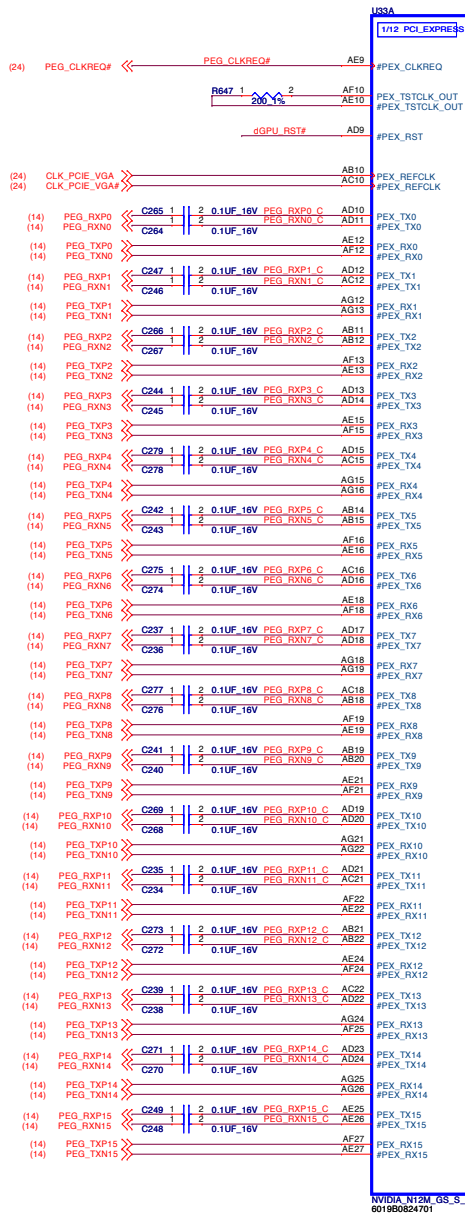
## Bluetooth CNN.



## PCIE Mini Card(WLAN)

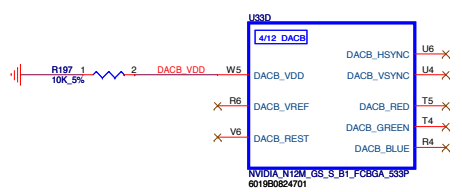
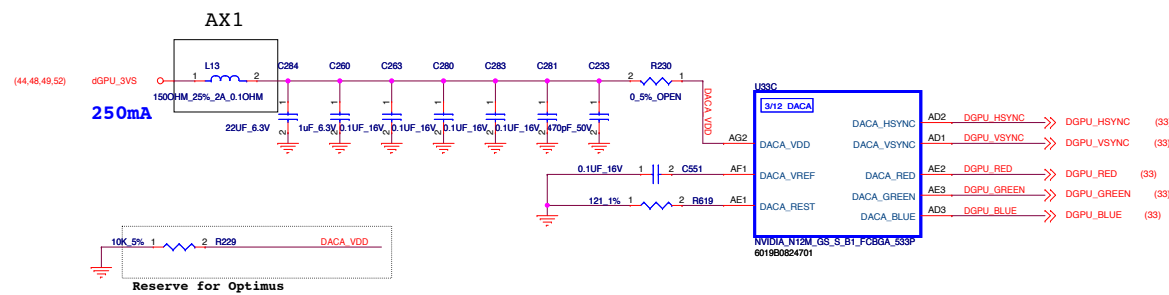
**INVENTEC**

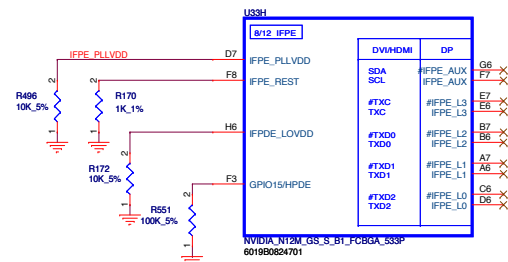
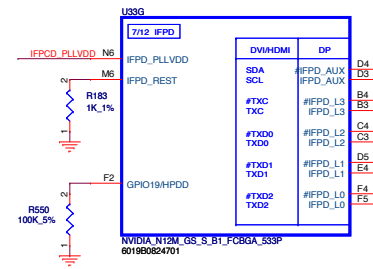
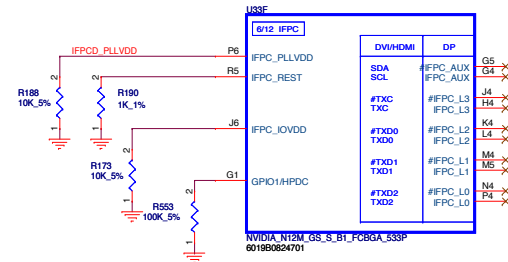
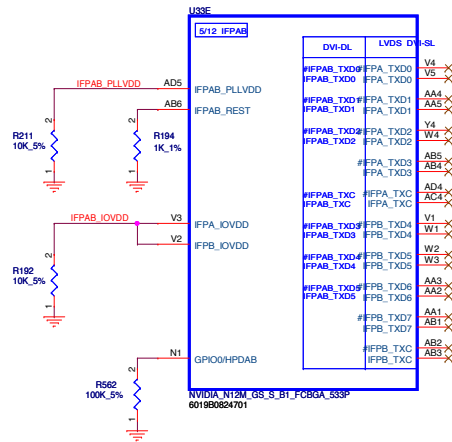
TITLE			
Strike WLAN/BT			
SIZE	CODE	DOC. NUMBER	REV
C	CS	CS-131	X01
SHEET		43 of	59

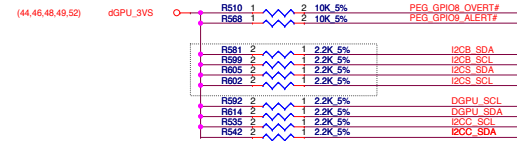
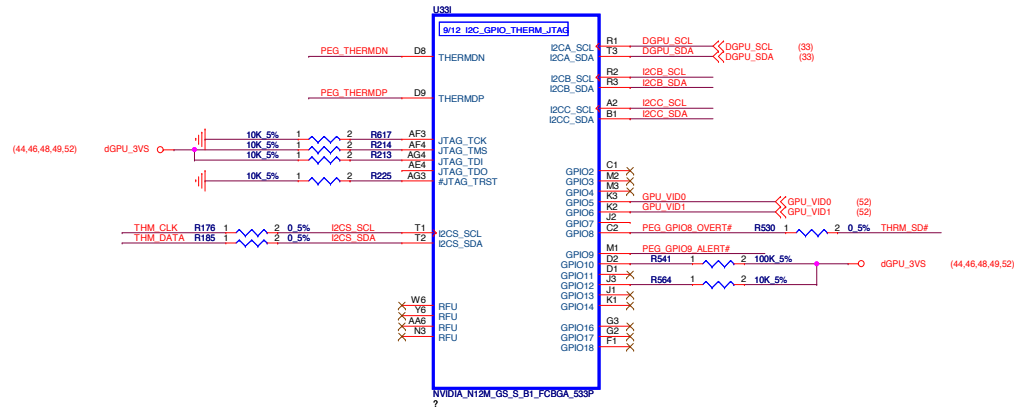


INVENTEC			
Strike			
N12M/PCI-EXPRESS			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	X02
SHEET	44	of	59



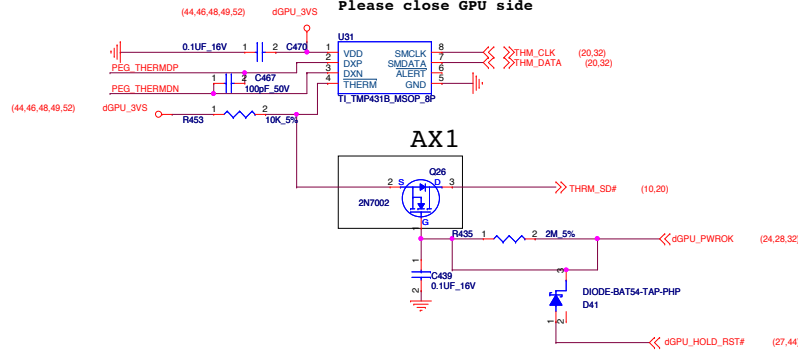






Reserve for Optimus

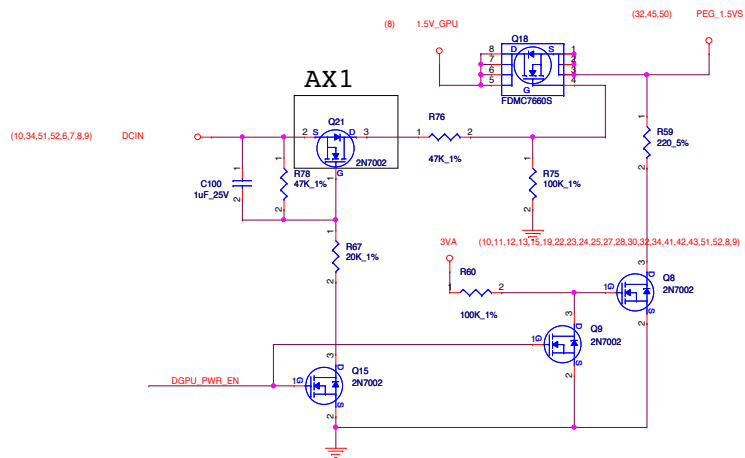
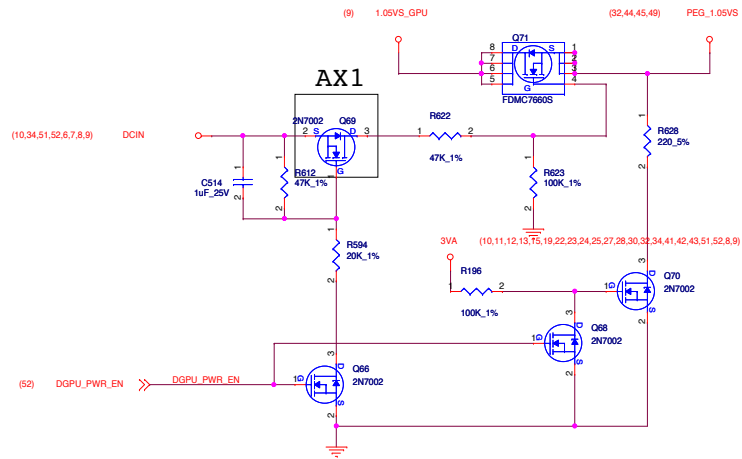
### GPU Thermal Sensor Please close GPU side













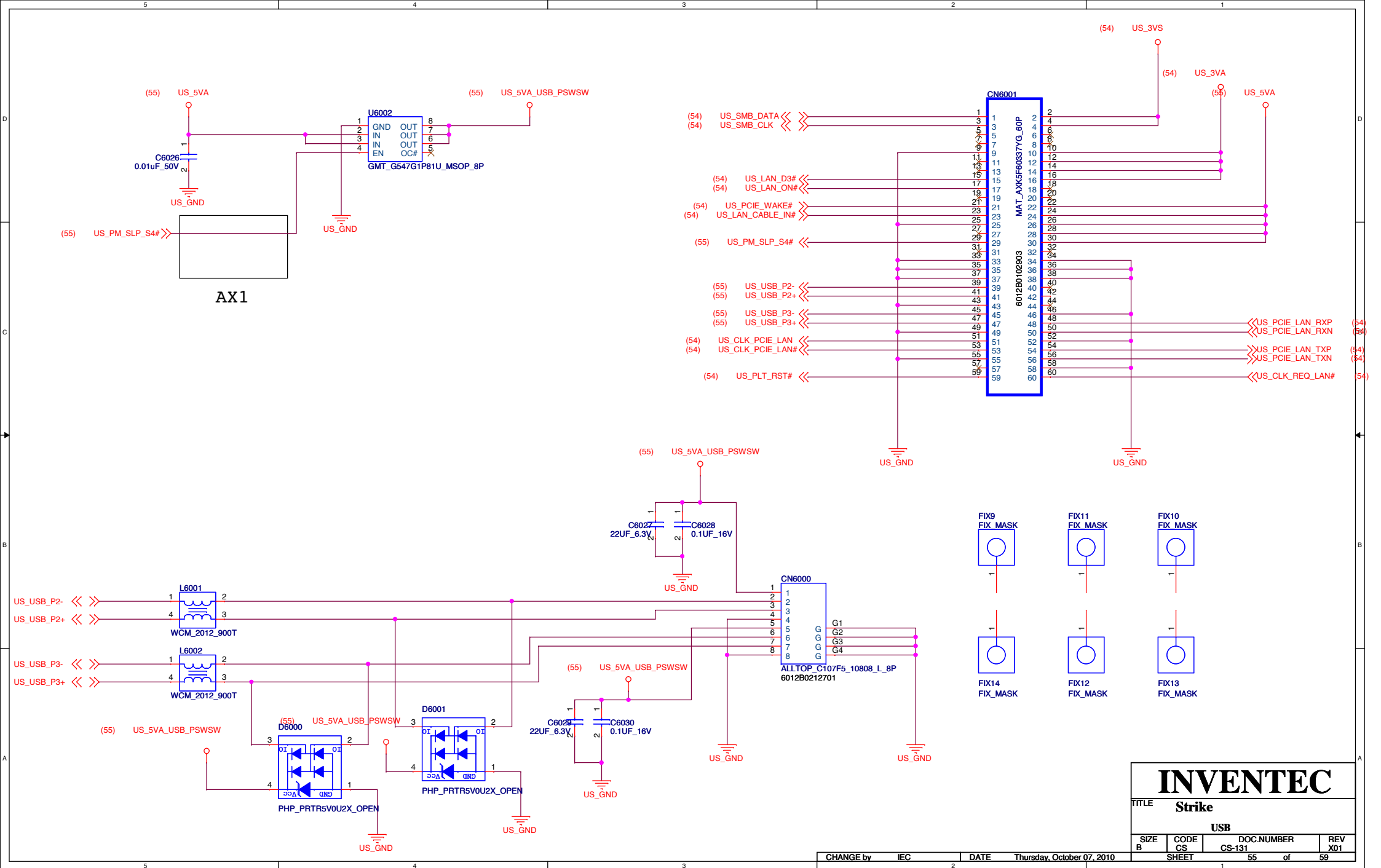
# Strike USB Board

2010.10.06

Thursday, Jun. 26, 2008	3'rd issue	AX1
Monday, May 26, 2008	Second issue	AX1
Thur., April 17, 2008	First issue	X01
DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	INVENTEC			
DESIGN					TITLE			
CHECK								
RESPONSIBLE					USB Board			
SIZE=					SIZE	CODE	DOC NUMBER	REV
FILE NAME XXXX-XXXXXX-XX					C	CS	K-CS-1310A22218-ALG	601
PIN XXXXXXXXXX					STREET		53	of 58





INVENTEC			
TITLE Strike			
USB			
SIZE B	CODE CS	DOC.NUMBER CS-131	REV X01
SHEET 1 of 59			

CHANGE by IEC DATE Thursday, October 07, 2010

# Strike

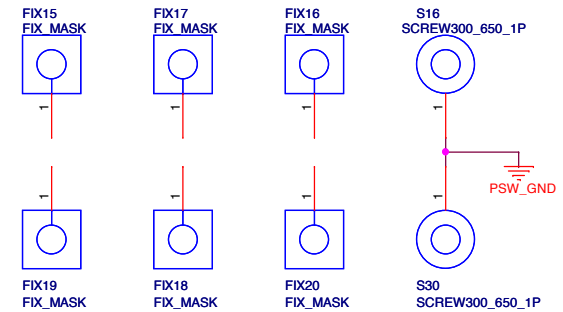
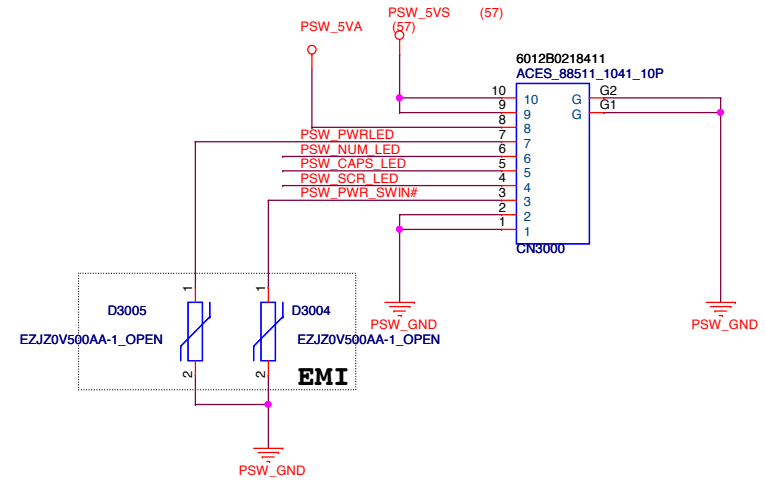
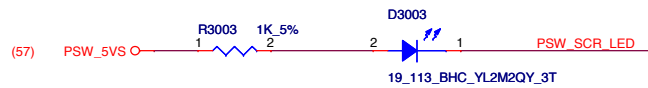
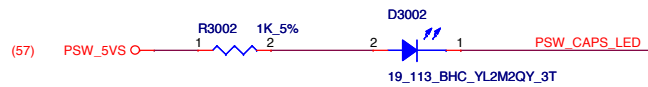
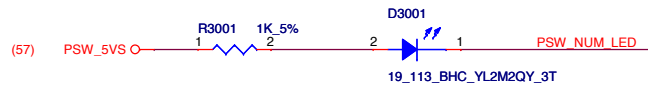
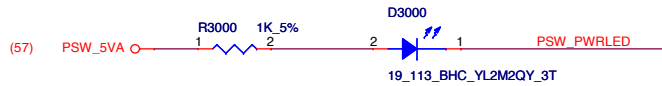
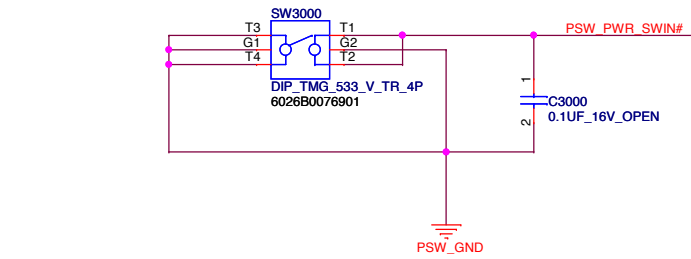
# PWR\_SW BOARD

2010.10.06

Thursday, Jun. 26, 2008	3'rd issue	AX1
Monday, May 26, 2008	Second issue	AX1
Thur., April 17, 2008	First issue	X01
DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	INVENTEC			
DESIGN					TITLE			
CHECK					PWR_SW BOARD			
RESPONSIBLE								
SIZE=					VER	SIZE	CODE	DOC NUMBER
FILE NAME XXXX-XXXXXX-XX						C	CS	K-CS-1310A22218-ALG
PN XXXXXXXXXX						SHEET	56	of 58





INVENTEC			
TITLE Strike			
Power Switch			
SIZE	CODE	DOC NUMBER	REV
B	CS	K-CS-1310A2219-ALG	B01
SHEET		57 of 59	

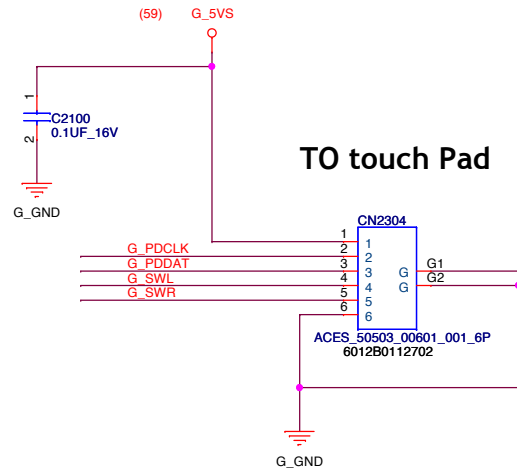
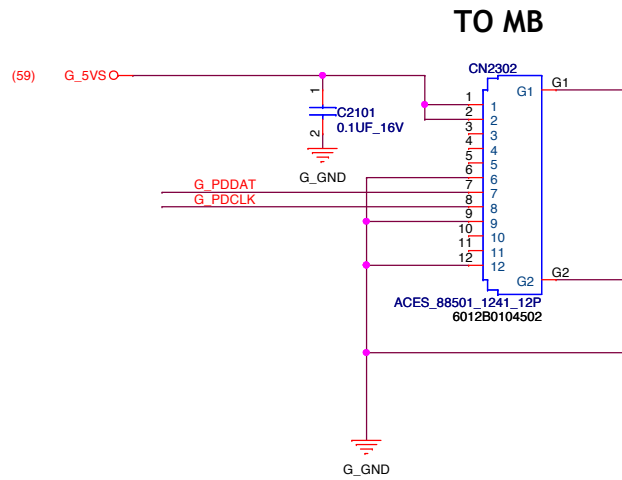
CHANGE by BEN LEE DATE Thursday, October 07, 2010

# Strike GP board

2010.10.06

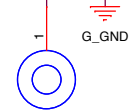
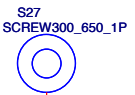
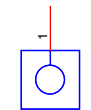
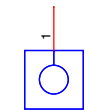
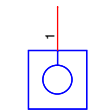
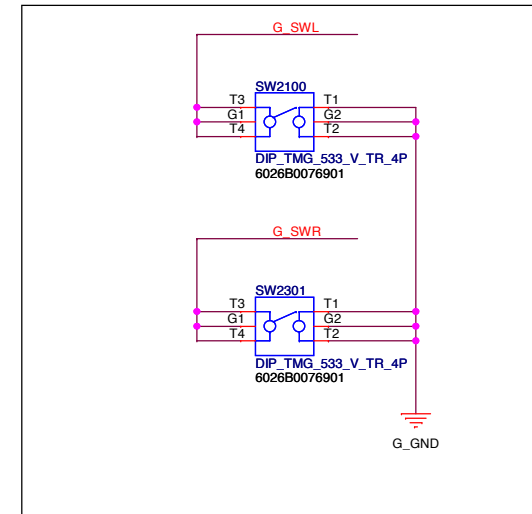
Thursday, October 07, 2010		
DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	<b>INVENTEC</b> Strike GP Board			
DESIGN								
CHECK								
RESPONSIBLE								
SIZE=					SIZE	CODE	DOC NUMBER	REV
FILE NAME XXXX-XXXXXX-XX					C	CS	K-CS-1310A22489	B
PIN XXXXXXXXXX					STREET	58	01	59



AX1

## GP Button



# INVENTEC

TITLE **Strike**  
**GP CNN**

SIZE B	CODE CS	DOC NUMBER K-CS-1310A22499	REV C
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CHANGE by	BEN LEE	DATE	Thursday, October 07, 2010
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SHEET 59 of 59